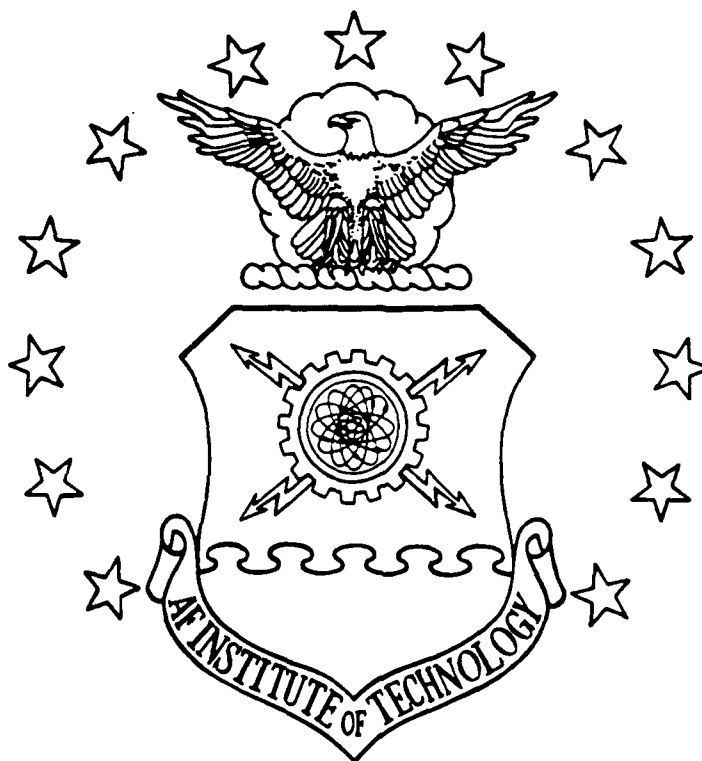AD-A215 352

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THE REDESIGN OF A MULTIELECTRODE
SEMICONDUCTOR ARRAY INTENDED FOR IMPLANTA
INTO THE BRAIN OF A RHESUS MONKEY

THESIS

David P. Szczublewski

AFIT/GE/ENG/89D-55

DEPARTMENT OF THE AIR FORCE

AIR UNIVERSITY

AIR FORCE INSTITUTE OF TECHNOLOGY

Wright-Patterson Air Force Base, Ohio

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THESIS

Presented to the Faculty of the School of Engineering

of the Air Force Institute of Technology

Air University

In Partial Fulfillment of the

Requirements for the Degree of

Master of Science in Electrical Engineering

David P. Szczublewski, B.S.E.E.

December 1989

Approved for public release; distribution unlimited

Preface

This thesis is just the latest contribution to a ten year effort to design, fabricate, test, implant, and monitor a multielectrode semiconductor array capable of investigating the mysteries of the visual system contained in the brain.

I would like to thank my thesis advisor Dr. Matthew Kabrisky for the encouragement, motivation, and technical support he provided me throughout my work. I would also like to thank my thesis committee members, Major Edward Kolesar and Major Steven Rogers, for providing their technical comments and suggestions to the initial draft of this thesis.

I would also like to thank Mr. Don Smith and Mr. Bill Tropp of the AFIT materials processing laboratory for their technical assistance in operating the processing equipment required for this thesis effort. I would also like to thank my fellow students, especially Doug Ford, Tom Jenkins, Dan Gammon, Jenny Shin, and Steve Pavick, for accepting me as a friend even though I was merely a civilian.

Finally, I would like to thank my wife Kathy, and children Greg, Doug, and Kelly, for supporting me and tolerating the obnoxiously long hours of my work.

<div style="text-align: right;">David P. Szczublewski</div>

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Abstract

A 16 X 16 multielectrode semiconductor array, previously designed in NMOS technology and intended for implantation into the brain of a rhesus monkey, must be redesigned in CMOS technology. The multielectrode array, known as the AFIT brain chip, must also have its aluminum electrodes replaced with a corrosion resistant metal that is capable of withstanding a subsequent polyimide cure temperatures of $350^{\circ}C$. The possibility of depositing the corrosion resistant metal directly onto the aluminum electrode was investigated. The metals investigated were gold, platinum, silver, and nickel as a barrier metal for the previous three metals. The redesigned CMOS array was partially functional and preliminary results from the metal study indicate gold on aluminum with a nickel barrier between them as the most promising electrode replacement. Further work in this area is continuing.

THE REDESIGN OF A MULTIELECTRODE SEMICONDUCTOR ARRAY
INTENDED FOR IMPLANTATION INTO THE BRAIN OF A RHESUS MONKEY

I.   Introduction

For the past ten years, graduate students at AFIT have been attempting to design, fabricate, test, and implant a multielectrode array capable of monitoring the visual cortex in the brain of higher order mammals. The multielectrode array, commonly referred to as the "brain chip", is designed by utilizing semiconductor technology to monitor the electrical signals of the visual centers in the brain by physically making contact with the brain. The approach used at AFIT is unique, and therefore, most of the available information is contained either in past AFIT theses or in journal articles written by AFIT personnel.

Background

Man has been fascinated for centuries as to how the human visual system works. The optical operation of the human eye, which images the visual stimuli on the retina, is well-documented and understood. Unfortunately, once the visual data are input to the retina and submitted for

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processing by the central nervous system, little of the actual brain processes and interpretion are understood. One proposed model, theorized by Kabrisky and others, suggests that bundles of neurons, the "cortical column", work together as functional elements to comprise the basic computing elements of the brain. In the visual cortex, the portion of the brain that processes visual data, these columns of neurons measure about 50 to 100 microns in diameter and about 2000 to 2100 microns in length (1:40). If the electrical signals, referred to as electroencephalographic (EEG) signals, from the arrays of columns in the visual cortex could be monitored, it should be possible to determine and model how column arrays react to various visual stimuli. In order to realistically accomplish this objective, thousands of columns would have to be monitored simultaneously. As an initial attempt, Demott (in 1966) used a 20 X 20 array of end-polished wire electrodes to monitor column arrays in the brain of a squirrel monkey (2:17-21). His two most significant problems were fabricating his array of 400 individual wires and managing their respective outputs. An array containing thousands of wire electrodes would, for all practical purposes, be impossible. Therefore, a new monitoring technique is required.

First Generation Brain Chip

In 1979, Joseph Tatman designed and fabricated the first AFIT brain chip, a 4 X 4 multielectrode semiconductor array, using junction field effect transistors (JFET's). Tatman's design is shown in Figure 1. The gates of each of the four JFETs in a row were tied together and connected to one of the external multiplexer channels; the source of each JFET was tied to one of the array electrodes; and the drains of each of the four JFETs in a column were tied together and connected to one of the external recording channels. Therefore, when the gate of any JFET was "turned on", any signal present at the electrode for that particular JFET would conduct to the output. Unfortunately, the circuit did not function electrically because of several fabrication problems (3:9-11). The following year, Gary Fitzgerald refined Tatman's design and successfully fabricated an electrically functional array. Although the circuit functioned electrically, it failed after 30 seconds in a 0.9% saline bath test that was used to simulate the environment found in the brain (4:108). This result indicated that the chip was not adequately protected from the harsh environment found in the brain.

The next refinement of the AFIT brain chip was done by George German in his 1981 thesis research. German evaluated
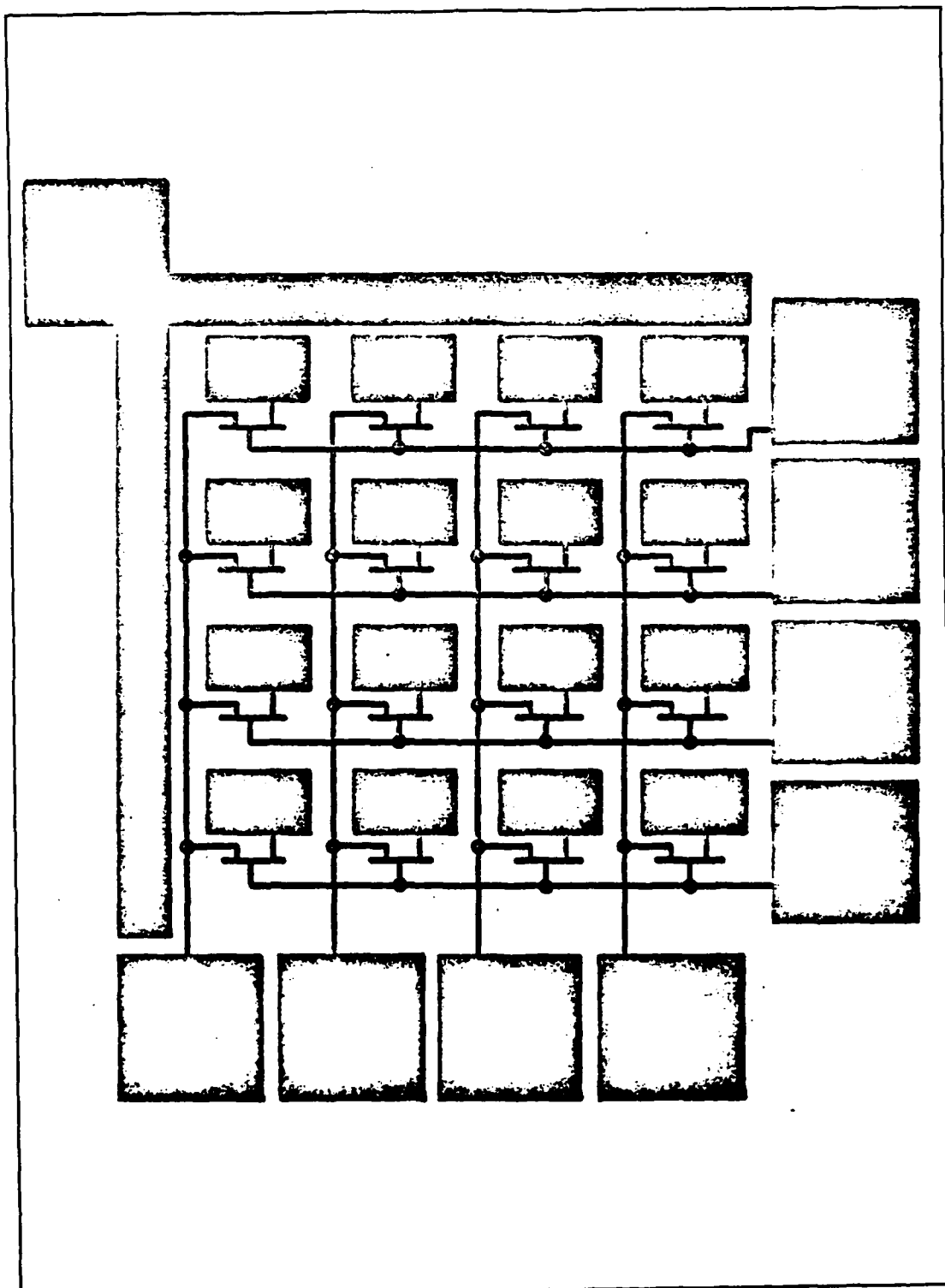
Figure 1. The 4 X 4 Multielectrode Array (5:12)

several materials for use as an encapsulant for the brain chip. The purpose of the encapsulant was to protect the JFETs from the contaminants that altered its electrical properties. Based on his test results, German recommended both phosphosilicate glass (PSG) and polyimide as possible encapsulants for the brain chip (5:59). The following year, Russell Hensley and David Denton made a major breakthrough. Based on German's results, they decided to use polyimide to encapsulate the 4 X 4 array and were able to surgically implant the chip into the brain of a dog. The chip was in the dog's brain for nineteen days and produced a tremendous amount of data. Analysis of the data indicated that EEG signals were being collected by the brain chip. Further detailed analysis with respect to the behavior adjacent cortical columns was inconclusive (6:92-93).

Second Generation Brain Chip

With the successful implantation of the 4 X 4 multielectrode array, a second generation brain chip was designed and fabricated by Robert Ballantine as part of his course work for a VLSI design course at AFIT (7:Appendix E). Ballantine's design, shown in Figure 2, was a 16 X 16 multielectrode semiconductor array that contained sixteen times as many electrodes as the previous 4 X 4 array, yet
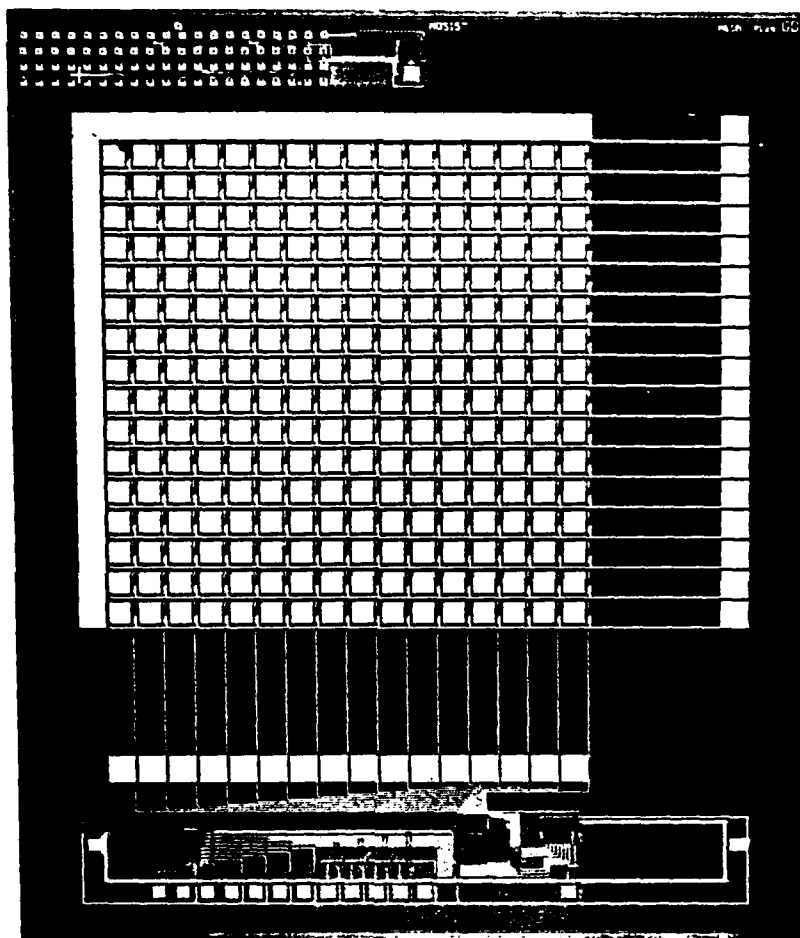
Figure 2. The 16 X 16 Multielectrode Array Designed by Ballantine (7:I-4)

was only one-fourth its size. Since the new array contained 256 electrodes, the rows of the array were multiplexed in groups of 16 in order to allow the time sequential output of all the gated electrodes on sixteen output wires. The new array was fabricated with NMOS technology. In 1984, Ricardo Turner did further research work on the 16 X 16 multielectrode array. He concluded that the NMOS brain chip was also extremely sensitive to the saline environment and that polyimide was once again an acceptable encapsulant for protecting the on-chip circuitry. Unfortunately, conventional NMOS manufacturing technology uses aluminum metallization (the AFIT JFET's used gold) and the saline solution rapidly deteriorated the aluminum pads (7:Section VI-1).

In 1986, Steven Ernst reevaluated polyimide (Du Pont PI-2555) and two polysiloxanes (Accuglass 407 and Diffusion Technology U-1A) for use as an encapsulate for the brain chip (8:Section I,5). Once again, the polyimide exhibited superior properties in comparison to the two polysiloxanes, and this material was recommended by Ernst (8:Section V,1).

Problem Statement

This thesis contains two major efforts. The first effort consists of redesigning, fabricating, and testing the

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16 X 16 multielectrode array brain chip. The most current

functional brain chip was designed by Ballantine in 1983 and

was fabricated with NMOS technology, which

characteristically uses only n-channel MOSFETs.

Unfortunately, NMOS technology is considered obsolete.

Current AFIT resources use only CMOS (complementary metal

oxide semiconductor) technology, which can use both n-

channel and p-channel MOSFETs. Therefore, the Ballantine

chip had to be designed using CMOS technology.

The second major effort consisted of an investigation

of platinum, gold, and silver as possible electrode

conductors. As previously discussed, the cerebrospinal

fluid (CSF) found in the brain is corrosive to the aluminum

electrodes used in the current Ballantine design. Obviously

the solution to this problem is to replace the aluminum

electrodes with a corrosion resistant metal that is

impervious to the CSF and have the brain chip fabricated

with such a metal. Unfortunately, CMOS technology, like

NMOS technology, dictates that the chip must be fabricated

with aluminum electrodes. Therefore, once the chip is

fabricated, the aluminum electrode must either be removed

and replaced with a corrosion resistant metal, or a

corrosion resistant metal must be deposited directly on the

aluminum electrode itself. This research effort will

investigate both possibilities by using gold, silver, and

platinum as the corrosion resistant metal. The metal investigation will also include the characterization of two key properties:

1.) The adhesion of the corrosion resistant metal to silicon dioxide and aluminum. Since the corrosion resistant metal must be deposited on aluminum and/or silicon dioxide, it is imperative that the metal adhere to these surfaces.

2.) The effect of the polyimide curing temperature has on the corrosion resistant metal-aluminum interface. Polyimide is used as an encapsulant of the brain chip and must be applied to the chip after the aluminum electrodes have been replaced or covered. If the corrosion resistant metal is deposited directly on top of the aluminum electrodes, it is quite possible that the subsequent polyimide cure temperature could accelerate intermetallic reactions between the metals and drastically change the electrical characteristics of the new electrodes. Therefore, the new corrosion resistant electrodes cannot be negatively affected by the polyimide curing temperature.

Assumptions

As a result of resource and time constraints, the following assumptions have been made:

1.) Platinum, gold, and silver are corrosion resistant metals capable of surviving the brain environment. This assumption is based on the many uses of these metals in medical applications.

2.) All deposited metals will be sputtered and the effect of any contaminants introduced during the sputtering process can be neglected.

3.) The composition of the aluminum available in the laboratory is identical to the composition of the aluminum from the electrode on the brain chip. Therefore, aluminum that is deposited in the laboratory for test purposes will produce test results similar to the aluminum contained in the brain chip electrodes.

Approach

The approach to this research effort will be divided into two separate parts. The first part will consist of the

redesign, fabrication, and performance characteristics of a 16 X 16 multielectrode array using CMOS technology. The second part will consist of the formulation and implementation of a test routine to characterize the adhesion and temperature properties for this particular application.

Redesign of the Brain Chip. The chip will be redesigned using CMOS technology and will closely follow the approach in the Ballantine NMOS design. The layout of the chip will be designed by using Magic, a VLSI computer-aided design tool available at AFIT, and will be sent for fabrication through MOSIS, a microcircuit fabrication service utilized by the government. Fabrication will take approximately ten weeks and, once completed, the chip will be visually and electrically tested to verify proper operation.

Investigation of Adhesion and Intermetallics. The property of adhesion and the effects of intermetallics will be investigated by using three-inch silicon wafers, growing silicon dioxide on the wafers, and sputtering various combinations of aluminum, platinum, gold, silver, and nickel onto the wafer. All of the metals will be patterned by utilizing positive photolithography methods. Once patterned, the electrical resistance of the patterned metal will be measured and the wafers will then be exposed to the

polyimide curing time and temperature. The wafers will again be visually and electrically inspected to determine if any significant amount of intermetallic growth has occurred. The adhesion property of the metal will be checked before and after temperature exposure by using the tape test. The results of this test sequence should determine an optimum metal or combination of metals to be used as the electrodes on the brain chip.

Sequence of Presentation

The design of both Ballantine's chip and the redesigned chip will be discussed and compared in Chapter II. Chapter III contains background information concerning the replacement of the electrodes, sputtering, intermetallics, and the properties of the metals chosen. Chapter IV contains the test methods used to test the redesigned brain chip and the results that were obtained. Chapter V contains the test methods and results from the intermetallics and adhesion investigation. Chapter VI contains the conclusions and recommendations.

II. Brain Chip Design

The purpose of this chapter is to discuss in detail the design and operation of the redesigned brain chip. The revised design will first be partitioned into modules and discussed at a block diagram level. Each module will then be implemented at the gate level. Particular attention will be given to both the on-chip control circuitry and the electrode design. The revised design will also be compared to a block diagram of the Ballantine brain chip, and the major differences and similarities between the two will be documented. Finally, the last section will discuss the details concerning the final design and fabrication of the redesigned brain chip, which includes the identification of all of the input and output pads. Throughout this thesis, a high signal (logic 1) can be assumed to be 5 volts, and a low signal (logic 0) can be assumed to be 0 volts.

Revised Brain Chip Design

A block diagram showing the major cells of the new brain chip design can be found in Figure 3. The major cells are the counter, the row selector, the row driver, and the gate electrode circuitry. Assume that each cell has both power (VDD, +5 volts) and ground (GND, 0 volt) applied.

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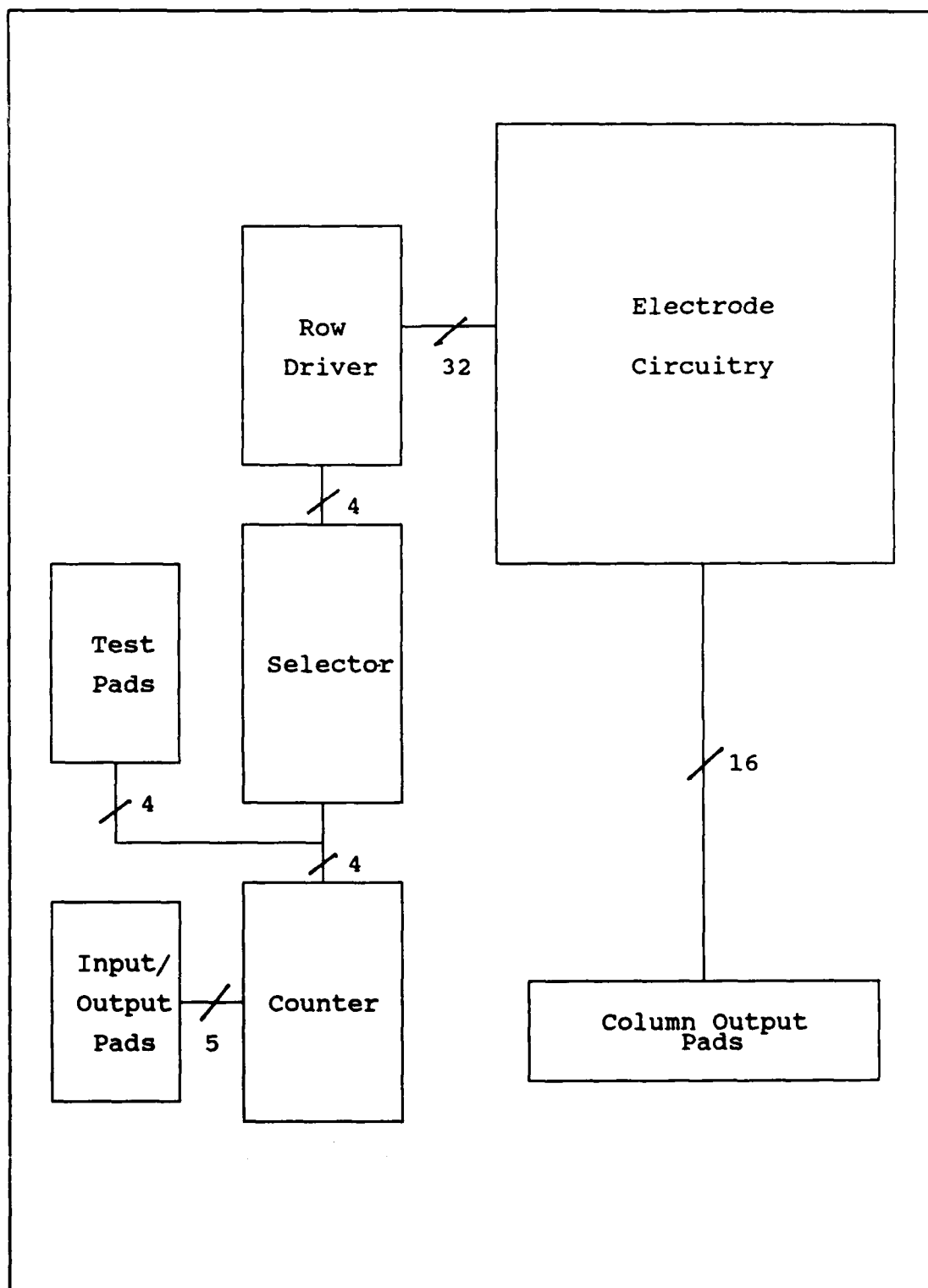
Figure 3. Block Diagram of the New Brain Chip

<u>Counter Operation</u> The counter is a modulo-16, four-bit counter that contains two inputs (RESET and CLK) and 5 outputs (RA0, RA1, RA2, RA3, and SYO). A description of each signal is contained in Table I. The counter is controlled by an external square wave clock generator. Basically, each time a clock pulse is detected at the clock input, the counter is incremented and outputs a new four-bit binary number. Once the counter reaches binary 1111, it automatically resets to binary 0000 at the next detectable clock pulse. The output signal SYO is the carry-out bit from the four-bit counter that is used to synchronize the counters on multiple brain chips.

Table I. Input and Output Signals for the Counter

RESET	resets counter to binary 0000
CLK	clock input
RA0	least significant bit (LSB) of binary output (2^0)
RA1	second-most LSB of binary output (2^1)
RA2	third-most LSB of binary output (2^2)
RA3	most significant bit (MSB) of binary output (2^3)
SYO	synchronization signal

<u>Counter Design</u> The counter was designed and simulated by Capt. Douglas Ford as part of his course work for a VLSI design course at the Air Force Institute of Technology, and a copy of his written report can be found in Appendix C.

<u>Row Selector Operation</u> The row selector contains four input signals (RA0, RA1, RA2, and RA3) and 16 output signals (SELECT_0 through SELECT_15). The four input signals, which originated from the output of the counter, are decoded and determine which row has been selected. Therefore, assuming the counter started at binary 0000, a pulse train of sixteen clock pulses input to the counter would result in SELECT_0 through SELECT_15 being selected sequentially through the outputs of the selector. The outputs of the selector employ negative logic, such that a selected output line is at a logic 0, while all other output lines are at a logic 1.

<u>Row Selector Design</u> The row selector was designed and simulated by Capt. Douglas Ford as part of his course work for a VLSI design course at the Air Force Institute of Technology, and a copy of his written report can be found in Appendix C.

<u>Row Driver Design and Operation</u> The row driver consists of sixteen identical subcells that contain two

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cascaded inverters. Each subcell, as shown in Figure 4, has one of the outputs of the selector as an input. Since the selector employs negative logic, the input signal is inverted to produce the output signal SELECT, and it is then inverted a second time to produce another output signal referred to as SELECT_BAR. Therefore, each subcell provides the drivers necessary to control the transmission gates contained in the gate electrode circuitry for a particular row of electrodes.

Gate Electrode Circuitry Design and Operation The gate electrode circuitry contains 256 identical subcells arrayed in a 16 X 16 matrix. Each subcell, as shown in Figure 5,
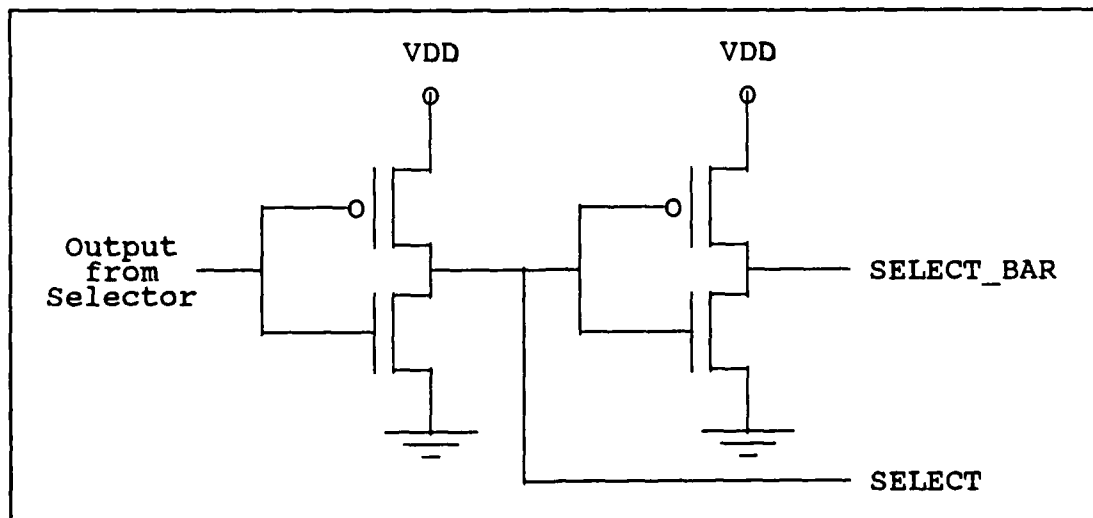
Figure 4. Subcell Schematic of Row Driver

contains one electrode and one transmission gate. The
transmission gate conducts when SELECT is logic 1 and
SELECT_BAR is logic 0. Therefore, for this particular case,
any signal present on the electrode will appear on the
column output bus. If SELECT is logic 0 and SELECT_BAR is
logic 1, the transmission gate is in a high impedance non-
conducting state, and any signal present on the electrode
will not appear on the column output bus. Since only one
row is selected at any given time, the column output bus
will only contain the electrical signal from the particular
row electrode selected.
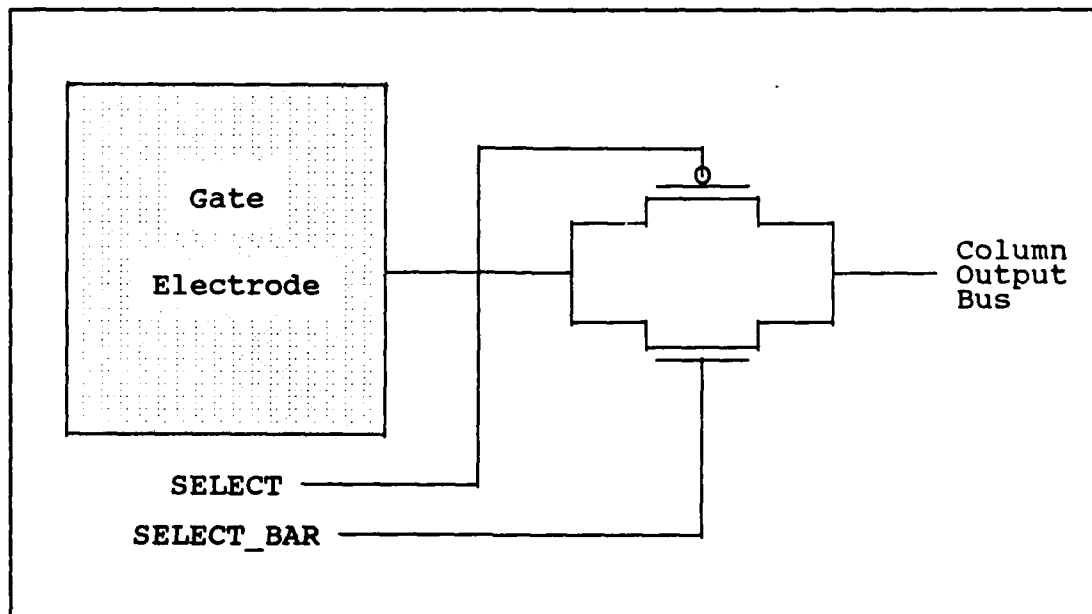
Figure 5. Subcell Schematic for the Electrode Circuitry

<u>Electrode Design</u> The size of the electrodes is 180 X 180 microns, which roughly corresponds to the size of the cortical columns in mammals, and the spacing between each electrode is 70 microns. Therefore, each of the 256 subcells contained in the array is 250 X 250 microns.

Ballantine Brain Chip Design and Comparison

A block diagram of the Ballantine brain chip design can be found in Figure 6. From an operational perspective, the new brain chip functions exactly like the Ballantine design except that the counter on the Ballantine chip was capable of eight different count sequences (7:Appendix F-4). The selected count sequence, as shown in Table II, was controlled by three inputs (CS0, CS1, and CS2). This allowed the Ballantine chip to monitor all, some, or none of the rows of electrodes depending on the particular count sequence chosen. The new design eliminated this feature since the same results can be obtained by manipulating the output data recorded from a fully operational array. The obvious benefit is the elimination of the three control inputs CS0, CS1, and CS2.
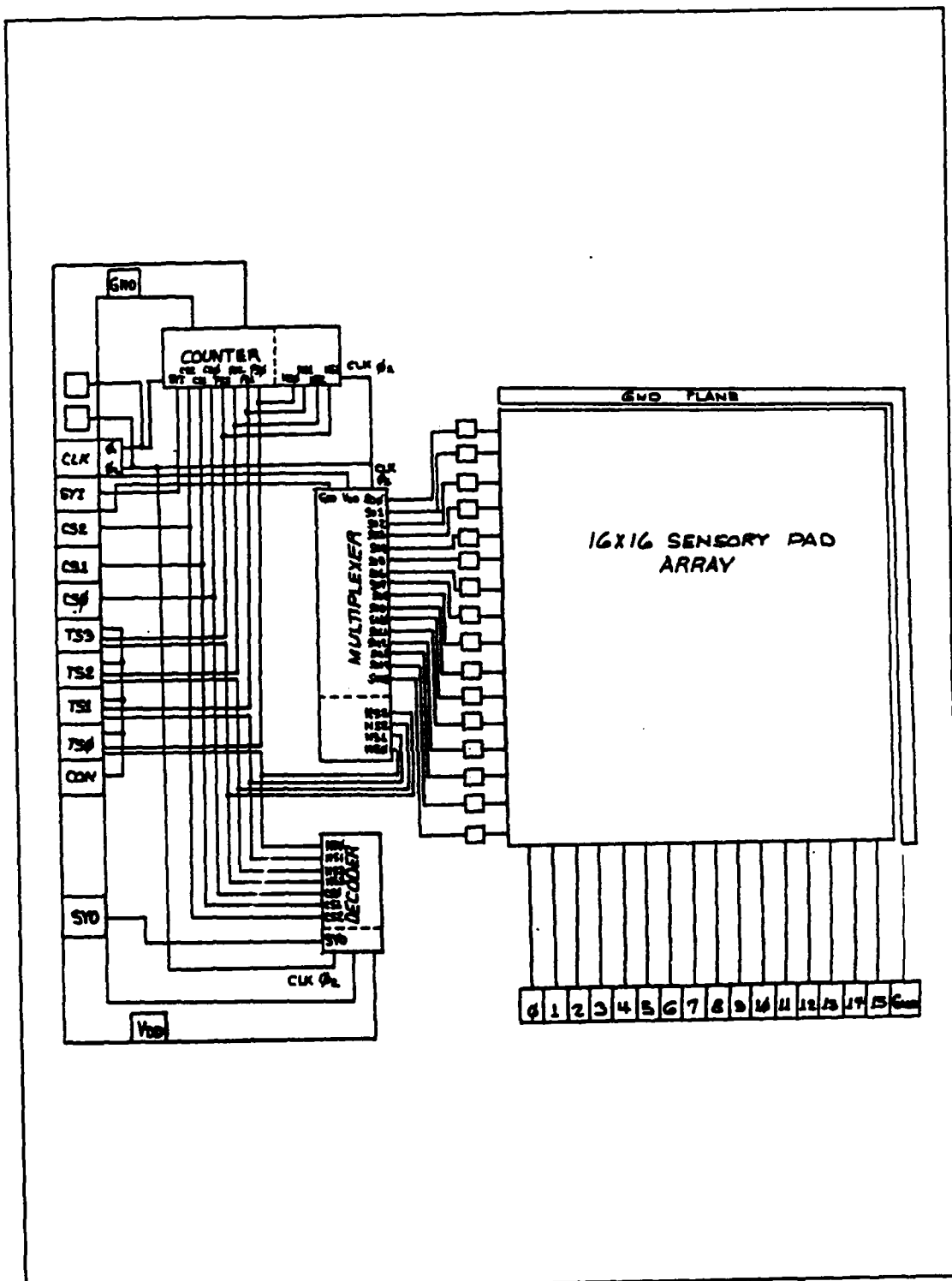
Figure 6. Block Diagram of Ballantine Brain Chip
(7:Appendix E,3)

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Table II. Count Sequence for the Ballantine Chip (7:E-6)

CS2	CS1	CS0	Counter Counts
0	0	0	0 to 15
0	0	1	0 to 3
0	1	0	4 to 7
0	1	1	8 to 11
1	0	0	12 to 15
1	0	1	0 to 7
1	1	0	8 to 15
1	1	1	0

Fabrication of the New Brain Chip

Each cell of the redesigned brain chip was individually designed with MAGIC, a computer aided design (CAD) tool used at AFIT for circuit layout. These cells were then incorporated into the brain chip design, along with the appropriate aluminum interconnections and input/output pads. The final brain chip design was electronically transmitted to the Metal Oxide Semiconductor Implementation Service (MOSIS) for fabrication into a 2 micron p-well double-level metal design rule technology. The fabricated chip, with all input and output pads identified, can be found in Figure 7.

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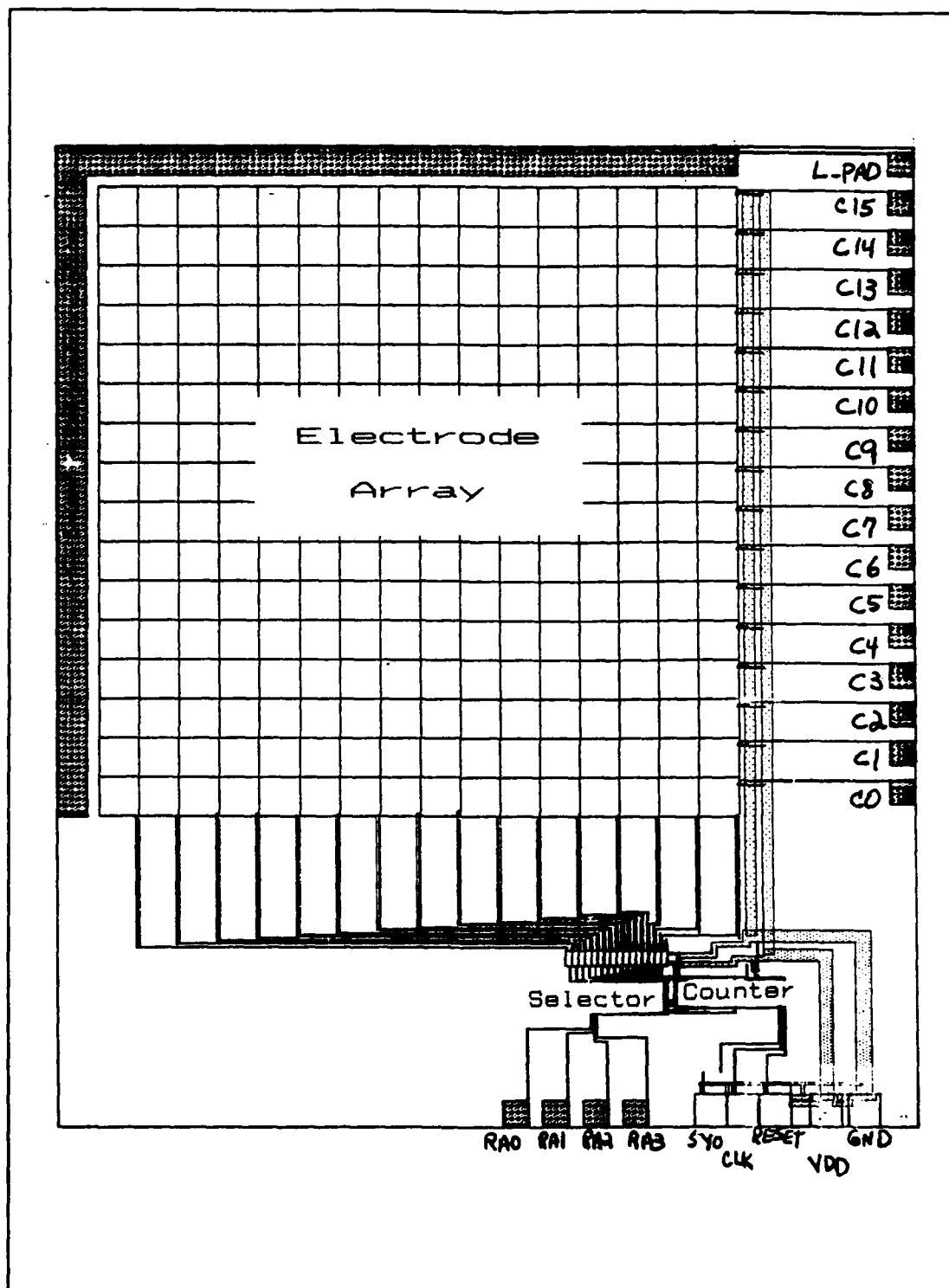
Figure 7. Redesigned Brain Chip With All Input and Output Pads Identified

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The new brain chip consists of four input pads (CLK, VDD, GND, and RESET), eighteen output pads (SYO, L_PAD, and C0 through C15), and four test pads (RA0, RA1, RA2, and RA3). A description of each can be found in Table III. The four test pads are only used during the initial electrical testing of the chip, and are capable of two separate functions: either to directly monitor the four-bit output of the counter or to input an externally generated count sequence into the selector circuitry. Therefore, if the chip doesn't function properly, it will be possible to determine whether the problem is with the counter or with the subsequent circuitry.

Table III. Description of the Input, Output, and Test Pads on the Redesigned Brain Chip

CLK	clock input into counter
VDD	voltage applied to chip (+5 volts)
GND	common circuit ground
RESET	resets counter to binary 0000
SYO	synchronization signal from counter
L_PAD	ground plane from the brain
C0 through C15	column outputs
RA0 through RA3	counter outputs

III. <u>Metal Theory</u>

The purpose of this chapter is to provide background information concerning the replacement of the aluminum electrodes, the sputtering deposition process, intermetallics, and the properties of the metals identified as a possible electrode replacement. The first section will discusses how the aluminum electrodes will be replaced. The second section discusses the sputtering deposition process, with particular interest in radio-frequency (RF) sputtering. The next section discusses what intermetallic compounds are and how they occur. The last section discusses the key properties of the metals chosen, which includes both electrical and physical properties.

<u>Replacement of the Aluminum Electrodes</u>

The aluminum electrodes must be replaced with a corrosion resistant metal. There are two ways that this can be accomplished:

1.) Remove the aluminum and deposit the corrosion resistant metal in its place. The only method of removal available at AFIT is wet chemical etching, a method that uses acids in their liquid form to selectively oxidize the

unwanted material (aluminum) and then dissolve the oxide into the liquid acid solution.

2.) Deposit the corrosion resistant metal directly on top of the aluminum.

Wet Chemical Etching Wet chemical etching was determined to be unacceptable since it would be extremely difficult to use wet chemical etching without seriously affecting the reliability of the entire circuit. Normally when wet chemical etching is used in the manufacturing process of integrated circuits to remove aluminum, it is performed immediately after the deposition process. A photoresist mask is deposited on top of the aluminum, and it is then patterned in such a way as to expose the desired aluminum to be removed. The photoresist mask, as shown in Figure 8A, is patterned by exposing the resist to ultraviolet light and developing the exposed region in a chemical solution, thereby opening a window that exposes the aluminum film to be etched. The circuit is then immersed into the acid solution to remove the aluminum. Aluminum etching, like most chemical etching, is isotropic, which means that the lateral and vertical etch rates are essentially the same (9:457). Therefore, as illustrated in Figure 8B, the etchant not only attacks the film exposed by
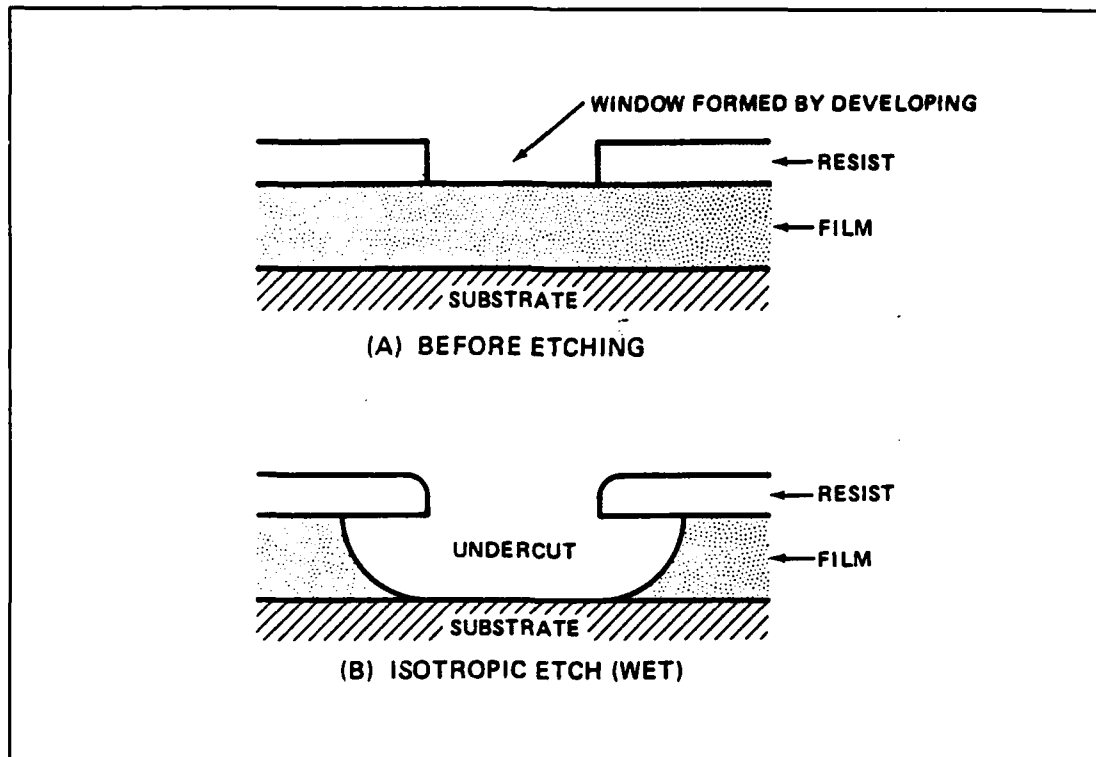
Figure 8. Example of Undercutting as a Result of Isotropic Etching (10:Chapter 9,5)

the window in the photoresist mask, but it also attacks the film beneath the mask. Once the desired aluminum is removed, the circuit must be rinsed in deionized water to stop the etch process. The remaining photoresist can than be removed, and the circuit is again cleaned in deionized water to insure that all residues from this process are removed from the surface of the circuit. The removal of surface contaminants is critical in order to prevent future chemical reactions that could be detrimental to the

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reliability of the circuit. Fortunately, once the photoresist is removed, manufacturers are capable of obtaining very clean surfaces since the isotropically etched surface on the chip should not contain any sharp corners to trap contaminants.

Wet chemical etching a fabricated circuit like the brain chip will increase the complexity of the process in the following ways:

1.) It will be difficult to size and orient the photoresist mask deposited on top of the chip. If the mask is too small or is not precisely aligned, it is very possible that the entire aluminum electrode will not be etched as desired.

2.) Undercutting under the glass passivation can occur, resulting in areas difficult to clean and metallize. A glass passivation is applied to the top of the chip after the aluminum is deposited, and windows are opened in it to expose the aluminum electrodes. This situation is analogous to the situation contained in Figure 8, except the photoresist layer is replaced by the glass passivation. Undercutting is not a problem when resist is used since the resist is removed after etching, thereby eliminating the source of the undercut. However, undercutting can be a

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problem with a passivated chip since the glass will not be
removed after etching. The undercut will be difficult to
clean as a result of surface tension from the contaminant(s)
within the undercut. Therefore, there exists a higher
probability that contaminants will remain after cleaning.
The undercut will also make it difficult to metallize as a
result of a shadowing effect. If the lateral undercut is
large and occurs at the output metal line of the electrode,
it is possible that the deposited corrosion resistant metal
would not make contact with the output metal line, thereby
isolating the electrode from the rest of the chip. The
undercut could also result in air bubbles being trapped
under the corrosion resistant metal which could expand under
thermal stress and break the corrosion resistant seal,
thereby creating a path for the contaminants.

Depositing Directly onto the Aluminum Electrode

Depositing the corrosion resistant metal directly onto the
aluminum electrode appears to be a better solution than
replacing the aluminum electrode. There still will be a
photoresist mask sizing and alignment problem with
metallization, but all of the problems associated with wet
chemical etching will be eliminated. There is a possibility
of intermetallics, but this problem is also possible with
the wet chemical etching solution since the corrosion
resistant metal will still have to come in contact with

aluminum. Therefore, assuming the effects of intermetallics are minimal, depositing the corrosion resistant metal directly onto the aluminum electrode should be a viable solution.

Sputtering

Sputtering is defined as the ejection of atoms from a surface as a result of surface bombardment by high energy atomic particles (11:91). These high energy particles, typically ions from an inert gas, collide with the surface atoms of the target material. If the surface atoms acquire sufficient energy via the collision processes, they are ejected from the surface, and the most probable direction of ejection is in exactly the opposite direction of the incident ion (11:92-95). The ejected atoms, each of which typically possesses a fraction of the energy from an incident ion, will strike any material in its path, transfer its energy, and accumulate on the surface of the material. The released energy is usually in the form of heat. The entire process is performed in a high vacuum, thereby significantly reducing the probability of the ions or the ejected atoms colliding with atmospheric gases (11:111-112). The most common methods of sputtering are DC, RF, and magnetron sputtering.

RF Sputtering The method of interest for this thesis

effort is RF sputtering. A typical RF sputtering system can

be found in Figure 9. The radio-frequency generator

operates at a frequency of one megahertz or higher; its

purpose is to generate a signal that counteracts the

positive charge that has accumulated on the surface of the

target. This positive charge is the result of the ion

bombardment of the target. The purpose of the adjustable

matching network is to match the load impedance with the

input impedance of the frequency generator. The blocking

capacitor prevents shorting the target to ground through the

matching network.
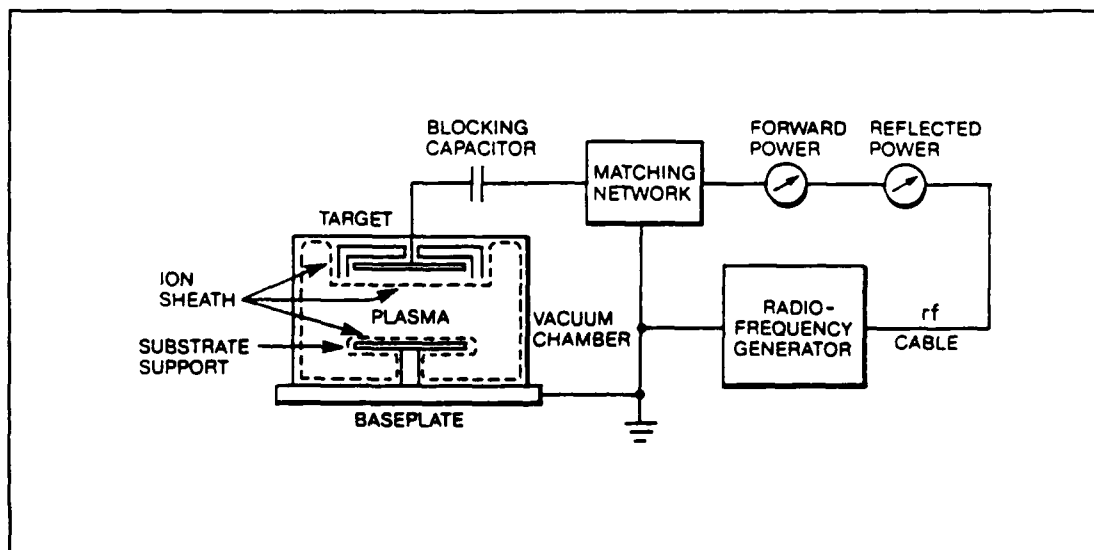
Figure 9. Radio-Frequency Sputtering System (11:125)

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Intermetallic Compounds

Intermetallic compounds are the compounds formed as a result of the reactions between two metals in contact with each other (12:190). There are three well-known types of intermetallic compounds; valency, electron, and interstitial compounds (13:42). Valency compounds are formed from metals that differ electrochemically. They obey the normal chemical rules of valency and are bonded together essentially by ionic or homopolar forces, or a combination of both. Electron compounds are formed from metals that are not markedly different electrochemically, but correspond to certain electron configurations. Interstitial compounds are formed from metals that have pronounced differences in atomic diameters. The smaller diameter atom of one metal is arranged between the spaces of the larger diameter atoms of the second metal (13:37-48).

The intermetallic compounds occur initially at the interface of the two metals and, as a result of the interdiffusion rates of the metals, can propagate within the metals themselves (14:128). The propagation of the intermetallic compounds can be accelerated by large time-temperature products since high temperatures usually increase the interdiffusion rates of the metals (14:128).

<u>Gold-Aluminum Interface</u> The most comprehensive intermetallic studies in the microelectronics industry have concerned the gold-aluminum interface. During the late 1960's and early 1970's, microcircuits that used gold bonding wires and aluminum pads were experiencing a significant number of failures as a result of open circuits occurring at the gold-aluminum interface. Typically, the failure mode was the gold ball bond lifting off the aluminum pad. Philofsky and others were able to show that five different intermetallic phases can occur at the interface. These phases could be distinguished by the aluminum and gold compound found ($AuAl_2$, $AuAl$, Au_2Al, Au_5Al_2, and Au_4Al) (15:1391-1392). Initially it was thought that one of the intermetallic compounds had a lower tensile strength than aluminum or gold, and thereby weakened the bond-pad interface, and that another intermetallic compound was nonconductive (16:Chapter 9,18). Philofsky was able to prove that the opposite was true: all five gold-aluminum intermetallic compounds had tensile strengths stronger than aluminum or gold and all were conductive (15:1397-1398). The real culprit of the bond failures was the degradation of the bond by Kirkendall voiding; that is, vacancies that are produced by unbalanced interdiffusion rates (14:128). Therefore, one of the metals was diffusing and forming intermetallics significantly faster than the other metal

could replace it. Philofsky was also able to show that the formation of Kirkendall voids was highly dependent on temperature and intermittent aging (15:1398-1399). At continuous temperatures above 300°C the formation of the voids was significant and greatly decreased the strength of the bond interface. However, intermittent temperatures even below 300°C also decreased the strength of the bond interface as a result of microcracks formed due to thermal expansion differences between the intermetallics of gold and aluminum (15:1398). These microcracks would serve as sinks for excess vacancies during subsequent temperature cycling, thereby accelerating the voiding process. The microelectronics industry greatly reduced this problem by developing lower temperature assembly processes that are performed after the gold-aluminum interface has been formed (14:128).

Conclusions from the Gold-Aluminum Interface The gold-aluminum interface demonstrates the effect that intermetallics and subsequent processing temperatures have on the interface's integrity. Therefore, in order to fully evaluate any metal-aluminum interface, it is important to simulate the interface at subsequent processing temperatures once the interface has been formed. This is an important point in the application of the brain chip electrode because the curing temperature of the polyimide used to passivate

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the chip is 350°C for 4 hours (8:C-2). Therefore, the possibility exists that the polyimide curing temperature could promote accelerated intermetallic growth and lead to the formation of Kirkendall voids. These voids could degrade the electrode in the following manner:

1.) Catastrophic failure as a result of an open circuit. If voids and microcracks are formed throughout the metal-aluminum interface, it is quite possible that no electrical connections exist at the interface.

2.) Catastrophic failure as a result of corrosion. The voids and microcracks would obviously degrade the adhesion of the metal to the aluminum and could compromise the integrity of the corrosion resistant metal seal. This would allow contaminants, such as the cerebrospinal fluid, to corrode the aluminum electrode and eventually lead to the catastrophic failure of the electrode.

Either of these possibilities would severely effect the electrical output of an implanted brain chip. Therefore, both must be avoided.

Metals Chosen

This section contains the key properties of the five metals chosen for this thesis effort: aluminum, platinum, gold, silver, and nickel. Aluminum will be used to simulate the aluminum electrode. Platinum, gold, and silver will be used as the corrosion resistant metal for the new electrode. Nickel will be used as a barrier metal between the aluminum and the corrosion resistant metal.

Aluminum Aluminum is the conductor of choice for use as interconnections on integrated circuits for the following two reasons (17:Section 2,21):

1.) Ease of processing. Aluminum is easy to deposit, primarily because of its low melting point ($660^{\circ}C$). This allows the integrated circuit to be processed at a lower temperature, thereby reducing processing defects. Aluminum is also easily patterned by chemical etching or reactive ion etching.

2.) Adherence to both silicon (Si) and silicon dioxide (SiO_2). Aluminum is one of the few conductors that will adhere to both Si and SiO_2, materials used extensively in the fabrication process.

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<u>Corrosion of Aluminum</u> One of the most significant
disadvantages associated with using aluminum as in the
metallization role in integrated circuits is its
susceptibility to corrosion (17:Section 6,34). By
definition, corrosion is the chemical attack of a metal that
takes place through the medium of water (10:451). Corrosion
can occur when there are at least two electrodes, some form
of electrolyte (water or water vapor), and some form of
ionic contamination. The rate and degree of corrosion is
dependent upon the amount of water available, the amount of
ionic contamination available, and the electrical bias
conditions (17:Section 6,34). Obviously, for the
application of the brain chip, extreme corrosion of the
aluminum electrode would be expected since the CSF would
have an ample supply of water and ionic contaminants (sodium
and potassium). This expected result has been substantiated
through previous AFIT thesis research by Turner (7:Section
VI,1).

Corrosion of the Aluminum-Metal Interface

Cathodic corrosion can occur as a result of voids between
the corrosion resistant metal and the aluminum brain chip
electrode (18:Volume 2;600). Table IV contains the standard
electrode potentials at 25°C for the metals of interest with
respect to hydrogen. From Table IV, it can be observed that
three of the selected metals (platinum, gold, and silver)

have large positive potentials with respect to aluminum. The larger the potential difference, the greater the possibility that cathodic corrosion can occur in the void. These potentials have the ability to essentially form a battery over a void and, if the void contains moisture and contaminants, can promote cathodic corrosion. For example, if platinum is deposited directly on top of aluminum, the potential that can exist between the two metals, under the right conditions, can easily promote corrosion. However, if a metal such as nickel was deposited between the platinum and aluminum layers, the potential would now be distributed between the two interfaces (aluminum-nickel and nickel-

Table IV.   Standard Electrode Potentials, Hydrogen Scale, 25°C (12:112)

Metal	Potential (Volts)
Aluminum	-1.67
Nickel	-0.25
Hydrogen	0.00
Silver	+0.79
Platinum	+1.20
Gold	+1.50

platinum) since, from Table IV, nickel is between aluminumand platinum. It should be noted that the voltage potentials contained in Table IV were measured under ideal conditions, with the pure metal sample immersed in an aqueous solution containing its own ions. Therefore, Table IV does not account for any compounds or oxides that could exist at the metal-aluminum interface that would affect the potential difference occurring at the interface (12:459-462).

Platinum Ideally, the use of platinum as an electrode material is desired because platinum is nonoxidizable, has a low electrical resistivity, has a stable electrical-contact resistance, and has an excellent resistance to corrosion (18:Volume 2;663). Unfortunately, platinum also has a high electrode potential with respect to aluminum and, with the two metals in contact, there is the possibility of a cathodic reaction occurring. Very little detailed information is available on the platinum-aluminum interface and at this time it is not known whether a cathodic reaction would occur in this particular application.

Gold Gold is another metal that could possibly be used as an electrode. Gold, like platinum, also has a high electrode potential with respect to aluminum and can have cathodic reactions at the gold-aluminum interface.

Silver Silver also has excellent corrosion resistance and is commonly used in medical applications. Turner attempted in his 1984 thesis to evaporate silver directly onto the aluminum electrodes of the Ballantine brain chip and was unsuccessful. The silver lifted off the electrode when the positive photoresist was removed. Turner theorized that silver would not adhere to aluminum oxide, a native oxide that aluminum readily grows when exposed to the atmosphere (7:III,12-13). Based on these results, Turner made a second attempt at depositing silver onto the electrode. In this attempt, first aluminum and then silver was deposited onto the Ballantine brain chip without breaking the vacuum in the deposition process. Therefore, new aluminum would be deposited onto the aluminum oxide of the electrode and the silver would then be deposited on top of the new aluminum. Since the vacuum of the deposition process would not be broken, the new aluminum would not be exposed to the atmosphere, and therefore, would not grow aluminum oxide on its surface. This second attempt proved successful, which demonstrated that silver would adhere to aluminum that did not have its native oxide on its surface (7:III,12-14). Therefore (using Turner's results), in order to use silver, another metal capable of adhering to both aluminum oxide and silver would have to be deposited between the two metals.

<u>Nickel</u> Nickel was one of the metals chosen to be used between the platinum-aluminum and gold-aluminum interface for the following reasons:

1.) Nickel has a voltage potential that is between those of aluminum-gold and aluminum-platinum.

2.) Nickel is used extensively in the plating and electronics industry as a barrier metal.

<u>Key Properties of Metals Chosen</u> Table V contains some of the key physical and electrical properties of aluminum (Al), silver (Ag), gold (Au), nickel (Ni), and platinum (Pt).

<u>Interdiffusion Rates</u> A literature search for the interdiffusion rates for the various metals contain in this thesis effort resulted in little or no information. The most obvious reason for this lack of information has to do with the complexity of the intermetallic system. For example, as previously discussed, the gold-aluminum system has five different intermetallic compounds, each of which has its own interdiffusion rate. Therefore, in order to accurately model the gold-aluminum system, the interdiffusion rates of the five intermetallic compounds must be known. Of course, concentration levels for each

Table V. Key Physical and Electrical Properties of
the Five Chosen Metals (18:Volume 2)

Metal	Al	Ag	Au	Ni	Pt
Atomic #	13	47	79	28	78
Atomic Weight	26.98	107.88	197.0	58.71	195.09
Density (20°C) (g/cm^3)	2.699	10.49	19.32	8.902	21.45
Melting Point (°C)	660	960	1063	1453	1769
Thermal Conductivity (10°C) $[cal/(cm \cdot °C \cdot s)]$	0.53	1.0	.71	0.22	0.165
Resistivity (20°C) $(\mu\Omega \cdot cm)$	2.6548	1.59	2.35	6.84	10.6

metal and intermetallic compound must also be known, along
with the order that each metal-intermetallic and
intermetallic-intermetallic interface occurs. Include the
temperature sensitivity of the entire system along with any
contaminants that are present and it is easily seen why the
gold-aluminum system is difficult, if not impossible, to
model.

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Summary

The corrosion resistant metal that replaces the aluminum electrode must be capable of protecting the brain chip from the CSF without effecting the electrical performance of the chip. The best solution appears to be to sputter the corrosion resistant metal directly onto the aluminum electrode. Therefore, the corrosion resistant metal must be able to adhere to an aluminum surface. The corrosion resistant metal-aluminum interface must not be susceptible to the growth of intermetallics, especially during the curing of the polyimide. Possible corrosion resistant metals include platinum, gold, and silver, with the possible use of nickel as a barrier metal. All four of these metals will be investigated in this thesis effort.

IV. Chip Test Methods and Results

The purpose of this chapter is to provide the test methods and results from the redesigned brain chip. The first section contains all the visual inspections performed after the chips were received from MOSIS. The second section contains the packaging procedures used in preparing a chip for electrical testing, and the third section contains the electrical tests performed. All three sections contain their corresponding results, including detailed discussions on any unacceptable results.

Visual Inspections

An initial visual inspection was performed on the chip after it was received from fabrication. An informal visual inspection was also performed before, during, and after all electrical tests. The purpose of the visual inspections was to identify fabrication defects, design defects, and handling defects. Fabrication defects, such as missing cells, missing or incomplete aluminum metallization, gross dimension errors, and corrosion are most likely to occur. Design defects are defects that occur as a result of design implementation errors, such as missing cells, missing metallization, extra cells, and extra metallization.

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Handling defects are defects that occur as a result of damage to the chip before, during, or after all visual or electrical tests. Since a visual defect, such as missing metallization, could be either a design or fabrication defect, it is imperative that design information be available during visual inspection in order to determine the cause of the defect. For the purposes of this thesis effort, a block diagram and Caltech Intermediate Form (CIF) plot were used during the visual inspection. A CIF plot is a graphical representation of the chip design created from the actual file sent to MOSIS for fabrication. Therefore, both the actual design and intended design were available during all of the visual inspections.

Results Two major design errors were discovered during the visual inspections. The first design error was discovered during the initial visual inspection, and the second design error was discovered during a visual inspection performed prior to electrically testing the electrodes. During the initial visual inspection, it was discovered that three adjacent control lines were missing a segment as shown in the photograph contained in Figure 10. These three control lines are located between the selector and row driver (refer to Figure 3), and they control the selection of the top three rows of the array (ROW_0, ROW_1, and ROW_2). Initially it was believed that the error was a

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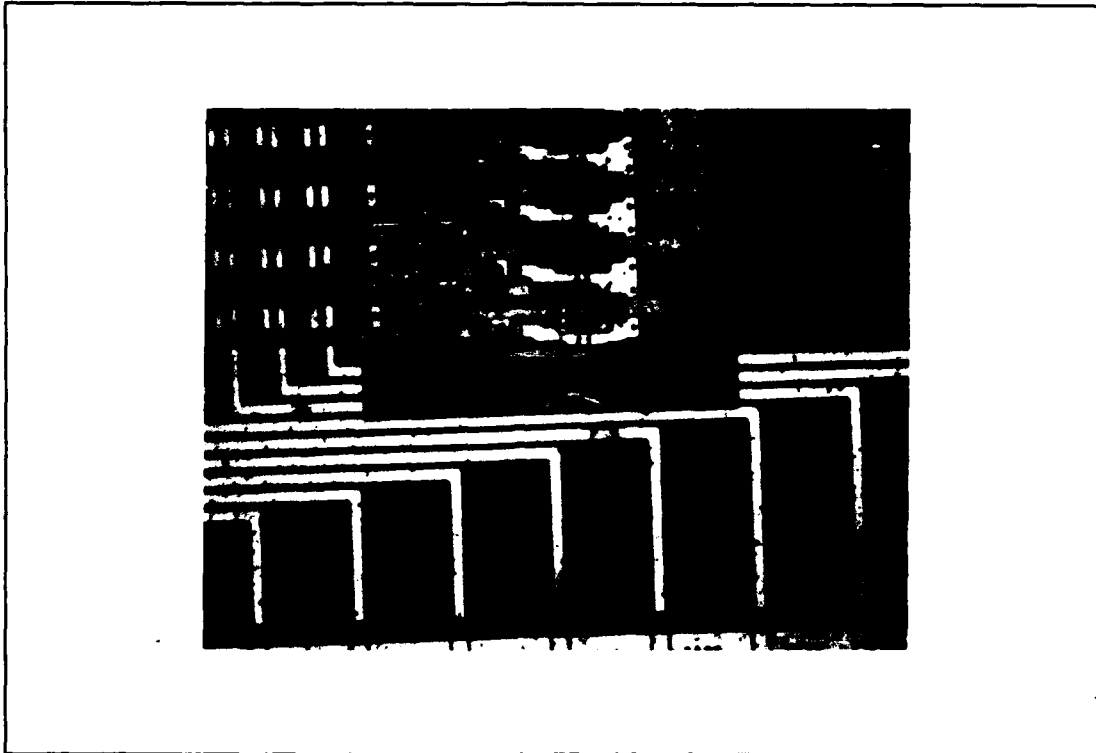
Figure 10. Photograph of Missing Control Lines at 250X

fabrication error since all control lines were verified
prior to submittal to MOSIS. However, examination of the
CIF plot indicated that the three control lines were missing
in the final design submitted to MOSIS. Therefore, it
wasn't a fabrication error but a design error. Further
investigation uncovered how such a gross design error could
occur. The final design submitted to MOSIS was the third
major revision of the new design. The first two revisions
corrected design errors discovered during simulation. An

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attempt was made to electronically submit the second revision to MOSIS for fabrication into a 2 micron n-well design. Examination of the CIF plot for this n-well design indicated that the three control lines were not missing. However, due to a computer problem with the electronic mail system, the second revision was not received by MOSIS in time to be included in the fabrication run. The next fabrication run for 2 micron n-well designs was scheduled for six weeks later, a length of time that was unacceptable. Fortunately, MOSIS had a 2 micron p-well design scheduled for fabrication two weeks later, a savings of four weeks. It was decided to convert the n-well design into a p-well design, a simple process since all of the cells, except for the input/output pads and electrodes, were designed to be fabricated in either an n-well or p-well process. The input/output protection pads were designed by MOSIS specifically for a 2 micron n-well design. Therefore, these pads were replaced in the third revision with input/output pads that were designed by MOSIS for a 2 micron p-well design. The electrodes in the second revision were designed, for isolation purposes, with a n-well underneath it. In order to maintain this isolation in the third revision, the n-well underneath the electrode was changed to a p-well. Once these two simple changes were made, the third revision was submitted to MOSIS for fabrication as a 2

micron p-well design. This revision was not resimulated
since the two changes were easily verified by visual
examination in MAGIC. However, as previously discussed, the
third revision was missing the three control lines.
Therefore, the three control lines had to be inadvertently
deleted during the third revision and, since the circuit was
not resimulated, the error was not detected.

A second major design error was discovered during a
visual inspection prior to the electrical characterization
of the electrodes contained in the array. The aluminum
electrodes were specified in the CIF plot with two aluminum
metallization layers. The physical structure consists of
the first layer of aluminum, a layer of insulation material,
and then the second layer of aluminum on top. The two
layers of aluminum are electrically connected through vias,
which essentially are small holes etched into the insulation
material prior to depositing the top layer of aluminum.
Therefore, the top layer of aluminum is deposited on both
the insulation material and any of the lower layer of
aluminum exposed through the via, and the topography of the
top layer contains a depression whenever a via occurs
(19:95). This effect is illustrated in the 500X photograph
of the aluminum electrode contained in Figure 11, where each
dot in the photograph represents a depression in the top
layer of aluminum as a result of a via in the insulation

47
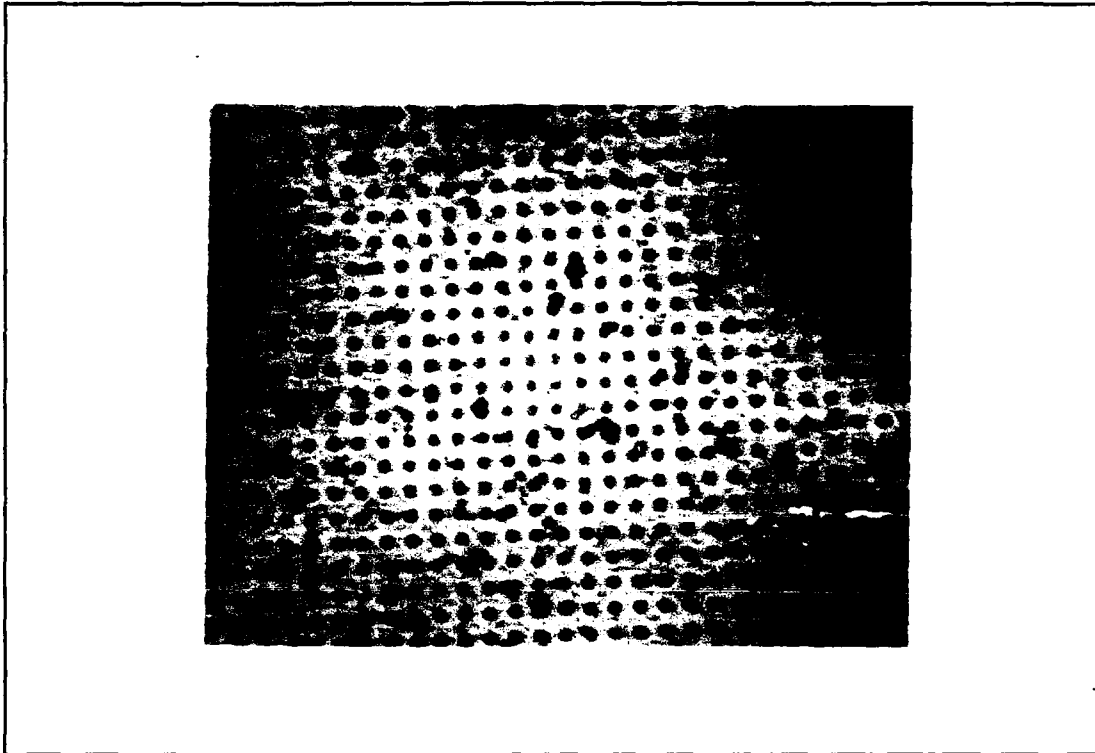
Figure 11. Photograph of the Aluminum Electrode at 500X

material. This effect is undesirable since the flattest

possible electrode surface required to couple the electrical

signal of the brain into the electrode has not been

obtained. A flatter surface can be obtained if just the top

level of aluminum is used as the electrode. The effect of

the vias were not realized during the chip design phase

since MAGIC does not display the vias on the computer

monitor.

Preparation for Electrical Testing

The chips were received from MOSIS in unpackaged form. Therefore. in order to electrically test a chip, it must be mounted in a package and wire bonded. The package used was a 64-pin dual in-line package (DIP). A silver-based conductive epoxy was used to mount the chip into the cavity of the DIP package. The conductive epoxy is a two part epoxy that consists of the silver paste and the hardener. Once the chip was mounted in the DIP package, an ultrasonic wedge bonder was used to attach aluminum wire from all output, input, and test pads to the package. The packaged chip must then be visually inspected for defects.

Procedure The following procedure was used to package a chip in a 64 pin DIP:

1.) Mix .5 grams of the silver paste with two drops of the hardener on a glass slide. Note that the epoxy mixture must be used within 30 minutes.

2.) Use the wooden end of a cotton swab to place a small amount of the conductive epoxy mixture in the cavity of the 64-pin DIP. The epoxy must be placed in the center of the cavity and cannot touch the sides of the cavity.

3.) Use tweezers to carefully place the chip in the cavity. The orientation of the chip should be determined from the chip wirebonding diagram. Gently press the chip down with a cotton swab until the epoxy in the bottom of the cavity is visible on all sides of the chip. The epoxy cannot touch the top of the chip or the sides of the cavity.

4.) Cure the epoxy by placing the DIP in an oven at $65°C$ for 1 hour. Once curing is complete, remove the DIP from the oven and let cool for 20 minutes.

5.) Wirebond all input, output, and test pads to the DIP with the ultrasonic wedge bonder in accordance to the wirebonding diagram contained in Figure 12.

6.) Remove the shorting bar from the pins on the DIP with wirecutters.

7.) Visually inspect the mounted chip and package for defects. Major defects include conductive epoxy on the chip, conductive epoxy on the DIP bonding pads, aluminum bond wire shorting to other wires or pads, bond wires unattached to the chip or DIP, or any other defects that could effect the reliability of the packaged chip.

Electrical Tests Performed

The packaged chip, shown in Figure 13, was electrically tested to verify its operation. The chip has been designed in such a way that the operation of the counter can be verified separately. After the counter has been tested, the row selector, row driver, and transmission gates will be tested as a group. The last electrical test will be the determination of the "on" resistance for the transmission gates. It can be assumed that VDD and GND was applied to the chip during the performance of all tests.

Counter Test Method The counter is controlled by two inputs, RESET and CLK. To test the operation of the counter, RESET was set high (+5V) to enable the counter and a 5-volt peak-to-peak 16 hertz signal was applied to CLK with a square wave pulse generator. The five counter

Figure 12. Wire bonding Diagram for Redesigned Brain Chip
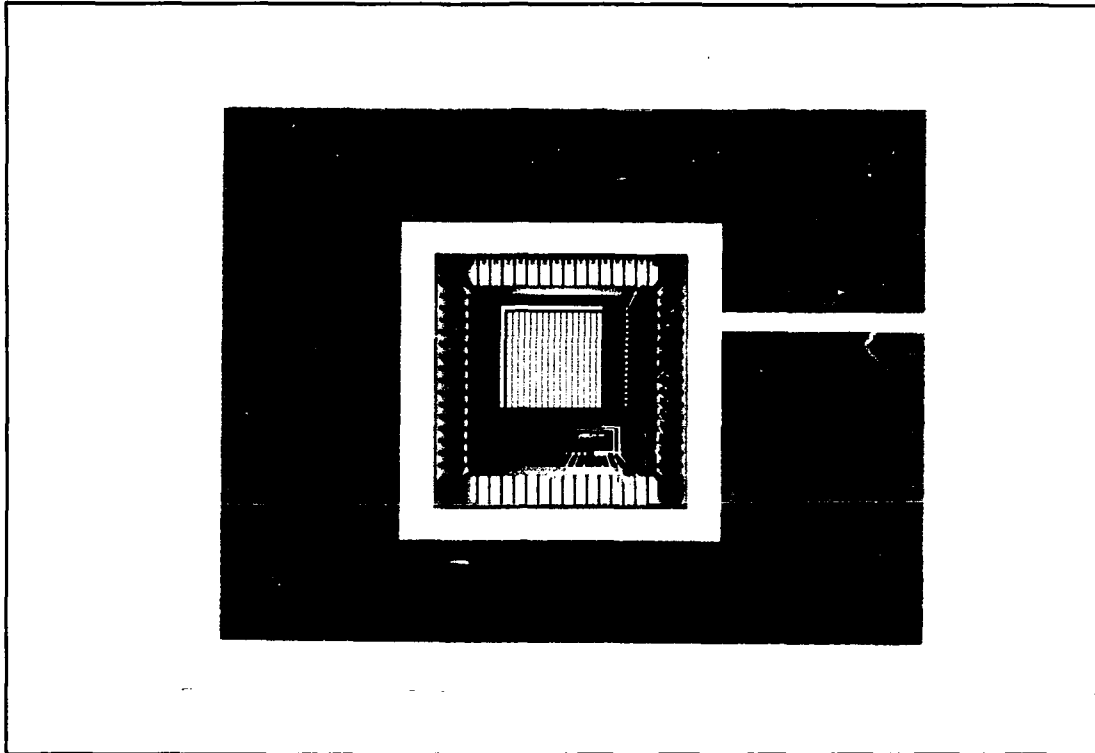
Figure 13. Packaged Chip in the Cavity of 64-Pin DIP

outputs RA0, RA1, RA2, RA3, and SYO were monitored with a digital oscilloscope.

    <u>Results of Counter Test</u> No significant electrical signals could be monitored on the five counter outputs. An ammeter on the power supply showed an excessive amount of current (1.4 amps) was being drawn from the power supply, an indication that a short to ground existed. This result occurred on four different chips that were tested. Examination of the MAGIC files did not show any obvious

shorts. Therefore, it was concluded that the counter does not function as a result of a timing problem.

Replacing the Counter The four test pads were designed into the chip in order to monitor the electrical outputs of the counter. However, if the output of the counter is isolated from the rest of the chip, it should be possible to use an external counter to input the required count signals into the selector through the four test pads. The four output lines of the counter, as shown in the 125X photograph contained in Figure 14, were severed with an ultrasonic cutter. A TTL synchronous modulo-16 binary counter (device number 74161) was selected as the external counter since most TTL outputs are capable of driving a CMOS input (20:Section 2,27). The electrical operation of the TTL counter was verified prior to its use (20:Section 4,221).

Selector Test Method Since the outputs of the selector can not be directly monitored, the selector, row drivers, and transmission gates must be tested as a group. The four outputs of the TTL modulo-16 counter, Q0, Q1, Q2, and Q3, must be hard-wired to the chip inputs RA0, RA1, RA2, and RA3 respectively (20:Section 4,221). A 5-volt peak-to-peak 16 hertz signal was applied to the clock (CP) on the TTL counter with a square wave pulse generator. A digital oscilloscope with a sweep speed of 100 milliseconds per

53
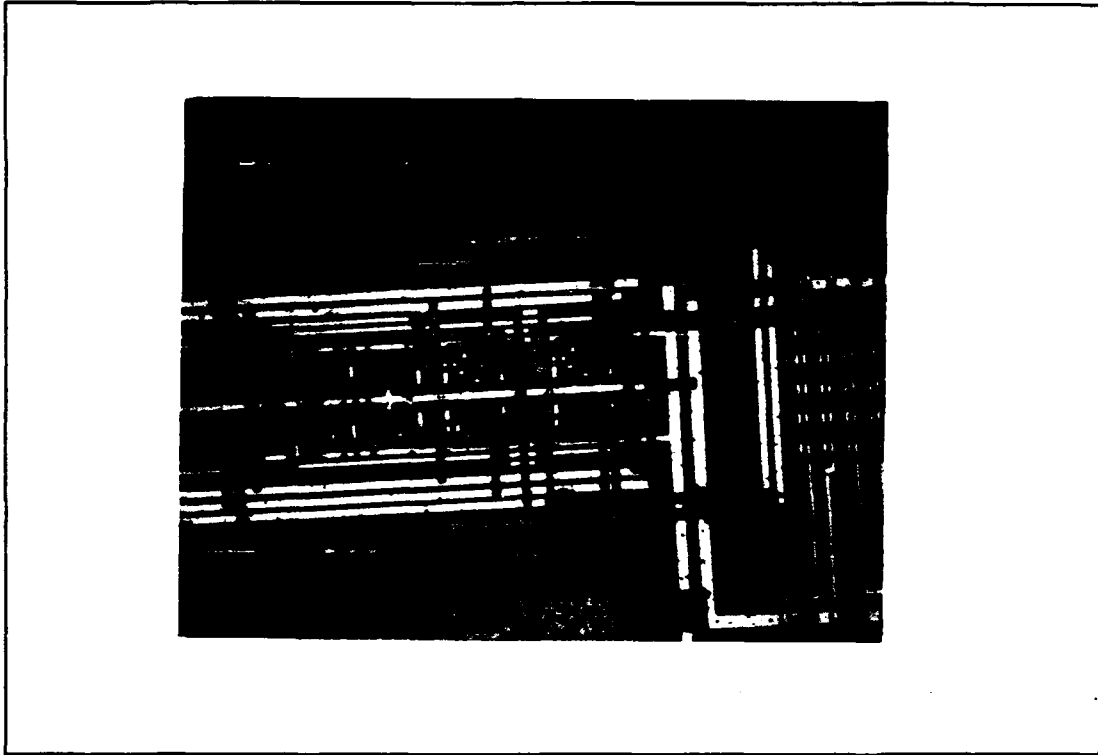
Figure 14. The Four Severed Output Lines of the Counter

division and triggered by the pulse generator monitored a

column from the array. Finally, a constant 1-volt signal

was sequentially applied to the electrodes in ROW_0 through

ROW_15 of the column being monitored by the digital

oscilloscope.

The purpose of the selector test was to cycle the TTL

counter (binary 0000 to 1111) once every second, trigger the

oscilloscope, and monitor the output from a column of

electrodes. Therefore, if a constant 1-volt signal was

applied to only one electrode in a particular column, the ideal output obtained from this column would be a single 1-volt square wave with a width that is one-sixteenth of the one second oscilloscope screen.

Results of Selector Test The results obtained from the selector test indicate that four of the sixteen rows of electrodes did not perform as expected. A constant 1-volt signal applied to any electrode in ROW_0, ROW_1, ROW_2, and ROW_4 resulted in a constant 1-volt signal on the output of the respective column. Therefore, the transmission gates for these four rows were always on. This result was expected for ROW_0, ROW_1, and ROW_2 since these are the control lines that were accidentally deleted prior to fabrication. However, the failure of ROW_4 was totally unexpected and cannot be explained. A visual inspection of the chip and an examination of the CIF plot and MAGIC file did not reveal any noticeable design or manufacturing errors. Time did not permit the resimulation of the selector, row driver, and transmission gate contained in brain chip design that was submitted for fabrication.

Figure 15 contains the output data from column C15 with a constant 1-volt applied to ROW_3. This procedure was repeated sequentially for ROW_5 through ROW_15 in column C15, and a similar pulse was obtain as in Figure 15 except the pulse moved to the right one pulse width at a time.
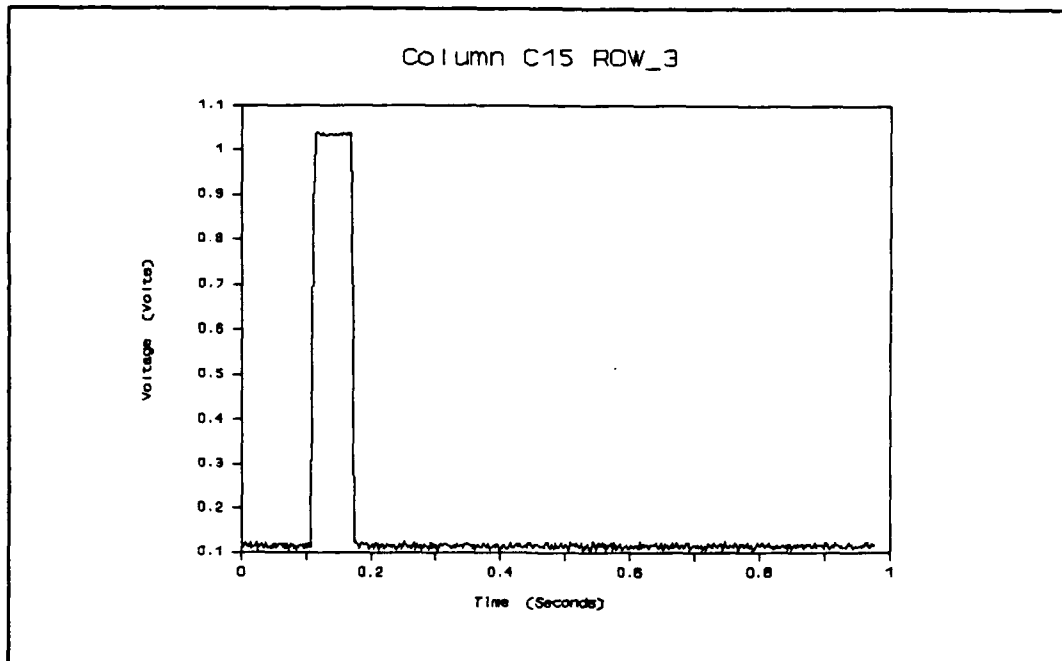
Figure 15. Output of Column C15 with 1-Volt Applied to ROW_3

Figure 16 contains the superposition of the output data of column C15 for ROW_3 and ROW_5 through ROW_15. It should be noted that the reference point for both Figure 15 and Figure 16 is approximately .1-volt. This is the result of the microscope light shining directly on the array. Three other columns (C0, C4, and C7) were tested in a similar fashion and the same results were achieved.

<u>"On" Resistance Test Method</u> One of the advantages of using the external TTL counter was that the outputs could be preset to a particular address. Therefore, it was possible

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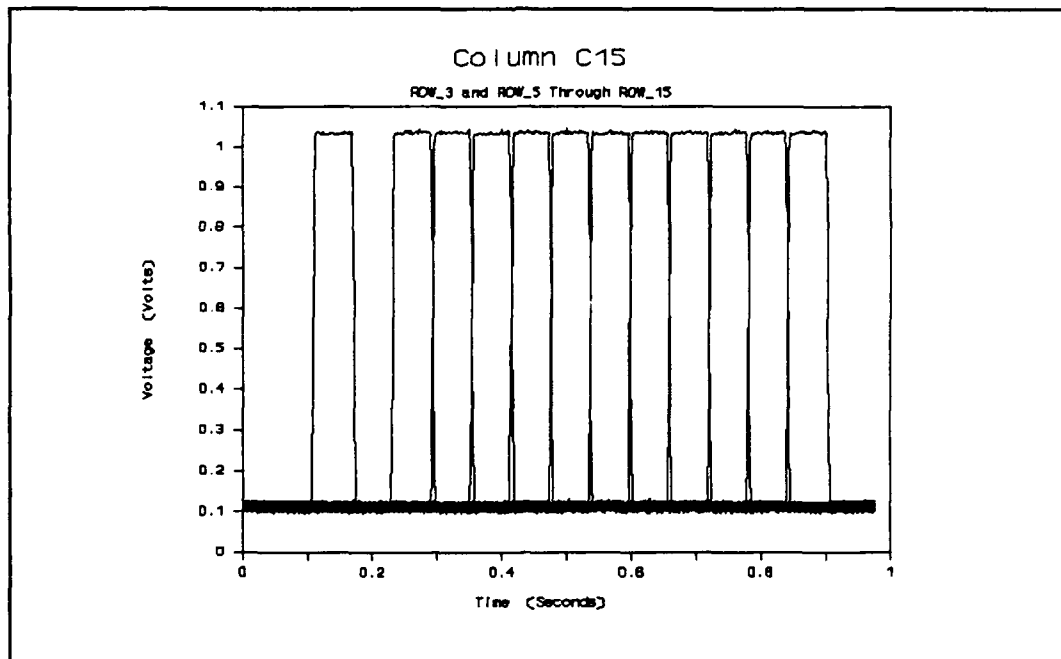
Figure 16. Superposition of the Output Data of Column C15 for ROW_3 and ROW_5 Through ROW_15

to continuously select the same row of the array. The preset address was applied to the TTL counter's four data inputs (A, B, C, and D), and ENABLE_T was set low in order to disable the count sequence (20:Section 4:221). A resistor was applied in series between the output of a column and ground. A constant voltage signal was applied to the selected electrode in the chosen column and a voltmeter monitored the voltage drop across the resistor. From this information, it can be determined what the voltage drop and resistance is from the electrode to the column output.

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Results of "On" Resistance Test   Table VI contains the results of the "on" resistance test obtained from applying different voltages (V) to the selected electrode. A 4.97K ohm series resistor was used and the measured voltage across it is V_1. The calculated current is I, and the calculated resistance of the electrode to the column output is R_{on}. All voltages contained in Table VI are in volts.

Table VI.   "On" Resistance Test Results

V	V_1	V_{Ron}	I (mA)	R_{on} (ohm)
.25	.219	.031	4.4×10^{-5}	703
.50	.415	.085	8.4×10^{-5}	1,018
1.0	.789	.211	1.6×10^{-4}	1,329
2.0	1.49	.510	3.0×10^{-4}	1,696

V. Metal Test Methods and Results

The purpose of this chapter is to describe the test methods and results of the metal study. The first section will discuss how the silicon wafers were patterned with metal, including photolithography and sputtering. The second section will discuss adhesion, including any visual inspections performed before and after all adhesion tests. The last section will discuss the electrical tests performed.

Patterning the Silicon Wafers

The patterning of the silicon wafers consisted of seven major steps:

1.) Preparation of wafers. The silicon wafers were first cleaned with Standard Clean #1 (described in Appendix B) to remove organic surface contaminates. After cleaning, approximately 5000 angstroms of SiO_2 was grown on the surface of the wafer in a dry oxidation furnace at $1050^{\circ}C$ for 30 hours.

2.) Apply and pattern the first level photoresist. The wafers were patterned with positive photoresist in accordance to Schedule #1 contained in Appendix B. The

photolithography mask was designed and fabricated following
Schedule #2 (described in Appendix B), and a photograph of
the mask is contained in Figure 17.

3.) Sputter aluminum onto the surface of the wafer in
accordance to Schedule #3 (described in Appendix B). The
thickness monitor must be calibrated prior to deposition
onto the patterned wafer.
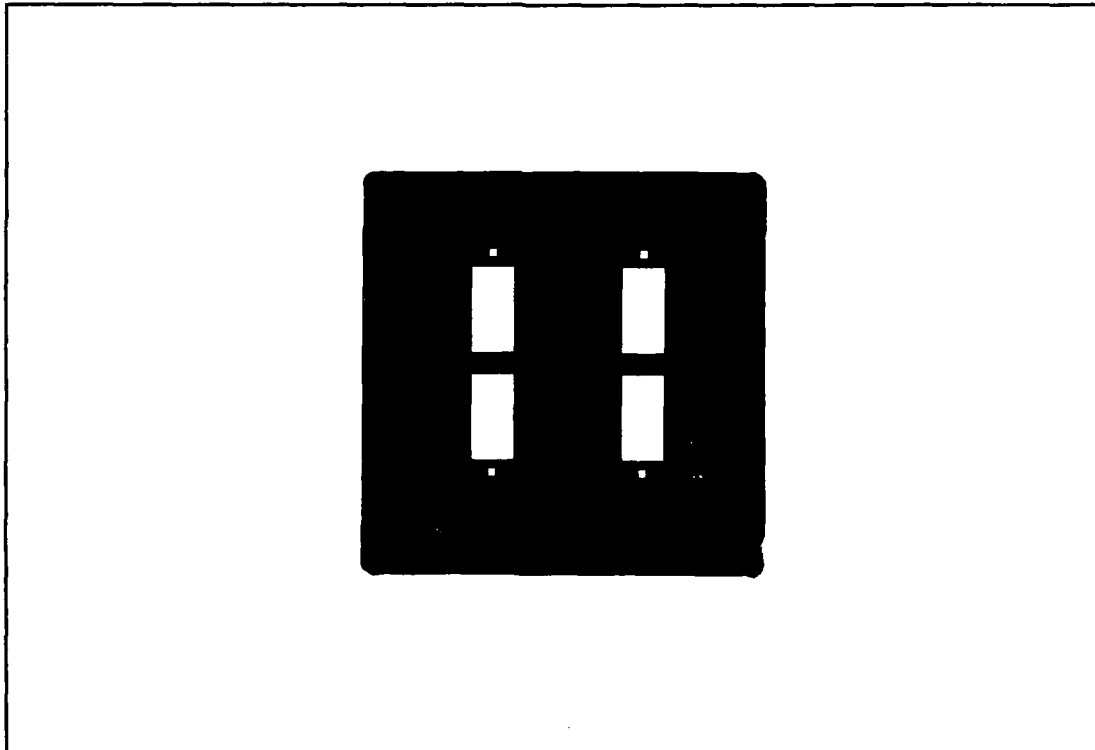
Figure 17. Photograph of the 4 X 4 Inch Photolithography
Mask Used to Pattern Both Photoresist Levels

4.) Remove remaining first level photoresist through lift-off. The metallized wafer was placed in a petri dish and covered with acetone. After 2-3 hours, the remaining photoresist lifted-off the wafer, thereby only leaving aluminum on the wafer where the windows in the photoresist occurred. The wafers were then cleaned in accordance with Standard Clean #2.

5.) Apply and pattern second level photoresist. The phototresist was applied, exposed, and developed according to Schedule #1, with the photoresist mask rotated 90 degrees prior to exposure to the ultraviolet light.

6.) Sputter barrier metal and/or corrosion resistant metal onto the wafer according to Schedule #3. If the second level consisted of two metals, the first metal (nickel or aluminum) was deposited and allowed to cool 20 minutes, then the second metal was deposited without the vacuum from the sputtering system being broken.

7.) Remove remaining second level photoresist through liftoff. The wafer was placed in a petri dish of acetone to promote the lift-off process. After the photoresist was removed, the wafer was cleaned according to Standard Clean #2. Figure 18 contains a photograph of one of the four identical patterns obtained on a wafer after the completion
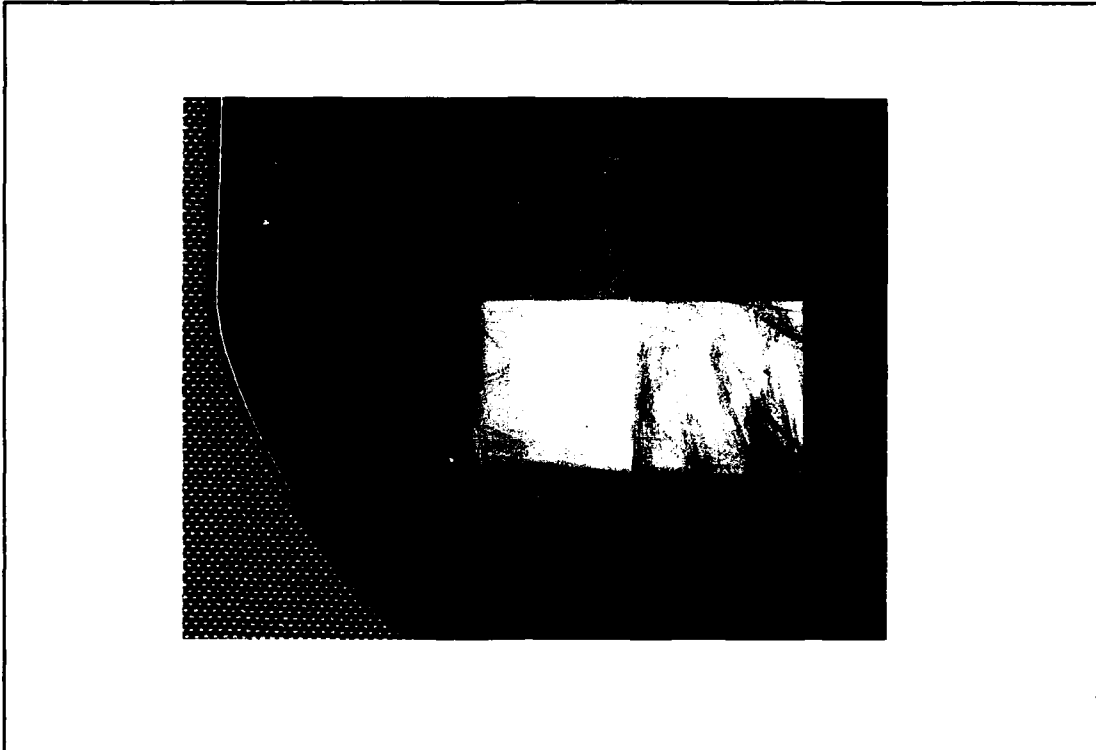
Figure 18. Photograph of One of the Four Identical Patterns Obtained on a Completed Wafer

of the second level lift-off. As shown by Figure 18, the L-shaped pattern was obtained by overlapping the level one aluminum layer with the level two barrier metal/corrosion resistant metal layer. The small squares were used to measure the thickness of each layer with the DEKTAK profilometer.

Problems Encountered During Patterning Two major problems were encountered during the patterning of the wafers with the different metal combinations. The first

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problem was the positive photoresist that was used would not completely lift-off in the acetone bath after the second deposition. The positive photoresist used has a final cure at 120°C. Literature indicates that substrate temperatures as high as 250°C can be obtained at high sputtering rates as a result of the heat energy released from the deposited metal (18:Volume 2). Therefore, high sputtering rates could over-bake and harden the photoresist, thus preventing lift-off. Since the sputtering rates initially obtained were approximately ten times as high for the corrosion resistant metals than aluminum, it was easy to understand why this problem was only occurring after the second level of metallization. To solve this problem, the sputtering rates were lowered by decreasing the RF power, rotating the table inside the chamber, and by taking "breaks" during long sputtering runs. This significantly reduced the problem but did not totally eliminate it.

The second major problem was again encountered during lift-off of the second layer of metallization. The corrosion resistant metal deposited on the SiO_2 would lift-off along with the positive photoresist. Therefore, only the second layer of metallization remained on the first layer of aluminum. All attempts to correct this problem by using different thicknesses and overdeveloping the photoresist proved fruitless. Therefore, it was concluded

that it was not a photoresist problem but an adhesion problem. The wafers would have to be used "as is".

High Temperature Exposure Test

The High Temperature Exposure (HTE) test consists of placing the completed wafers in a 350°C oven for two hours. The adhesion tape test and electrical resistance measurements were made before and after the HTE test. Since each wafer was fabricated with four identical patterns of metal, two of the patterns were used for the before and after adhesion test and the remaining two were used to obtain an average electrical resistance measurement. The adhesion test was considered a destructive test. Therefore, once a pattern of metal was used for an adhesion test, it was not used for any other test results.

Adhesion Test

The adhesion test consisted of applying a fresh piece of tape to the sample (one pattern of metal), firmly rubbing the tape into place with a cotton swab, and removing the tape by pulling it off as close to 180° as possible. The tape was examined to determine how much of the metal came off the aluminum intersection and the SiO_2, and the results were rated in accordance to the adhesion test rating system

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contain in Table VII. Before and after each adhesion tape
test, the sample was visually examined for signs of
corrosion, discoloration, and gross surface imperfections.

Table VII. Adhesion Test Rating System

100%	No second layer metal removed from sample
75%	75 to 100% remains
50%	50 to 75% remains
25%	25 to 50% remains
0%	0 to 25% remains

<u>Results of the Adhesion Test</u> The results of the
adhesion test before and after the HTE test can be found in
Table VIII. Several of the test samples that contained two
metals in the second layer showed adhesion problems between
the two metals and were so noted. A different pattern of
metal was used before and after the HTE test, therefore it
was possible for the second level metal(s) to have poor
adhesion prior to the HTE test and good adhesion subsequent
to the HTE test. Any obvious color changes that occurred
during the HTE test were also noted in Table VIII. An
adhesion test was not performed on the Au sample after HTE
since very little Au remained on the surface.

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Table VIII. Results of the Adhesion Test Before and After the HTE Test

Level 2	Before HTE Test		After HTE Test	
Metal(s)	Al	SiO_2	Al	SiO_2
Au	0%	0%[a]	---	---
Pt	100%	0%[a]	0%[b]	---
Ag	100%	0%	100%[c]	100%[c]
Pt on Al	100%	100%	0%[b,d]	0%[b,d]
Ag on Ni	75%	0%[d]	100%[c]	75%[c]
Pt on Ni	100%	0%	100%	0%
Au on Ni	100%	0%	100%	0%

[a] metal came off during lift-off

[b] Pt appeared dark gray in color

[c] Ag appeared bright yellow in color

[d] top metal in second level had 0% remain and bottom metal had 100% remain

Results of Visual Inspections   A visual inspection was performed under a microscope at 250X to look for any obvious signs of corrosion before and after the HTE test.

Gold   Figure 19a contains a 250X photograph of the level 2 Au sample before the HTE test. The bottom of the photograph was taken near an edge of the metal pattern to show that the photograph is in focus. Figure 19b contains a 250X photograph of the level 2 Au sample after the HTE test. Very little Au remained on the surface of the sample after the HTE test, and a blackish substance was visible on the areas where Au did not appear. As a result of time and equipment restraints, the blackish substance was not analyzed to determine its composition. However, it is obvious that some type of reaction had occurred, with intermetallic growth being the most likely cause.

Platinum   Figure 20a contains a 250X photograph of the level 2 Pt sample before the HTE test. Once again, an edge of the film pattern was used for focusing purposes. The bottom layer is the wafer, the middle layer is the aluminum, and the top layer is the Pt. The overlap of the aluminum is the result of a misalignment of the photoresist mask during level 2 deposition and should not have any effect on the HTE test. Figure 20b contains a 250X photograph of the level 2 Pt after the HTE test. The surface has become rough, with the grayish spots indicating that a reaction of some type has occurred.

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(a.)

(b.)

Figure 19. 250X Photographs of the Au Sample Before and After the HTE Test

(a.)
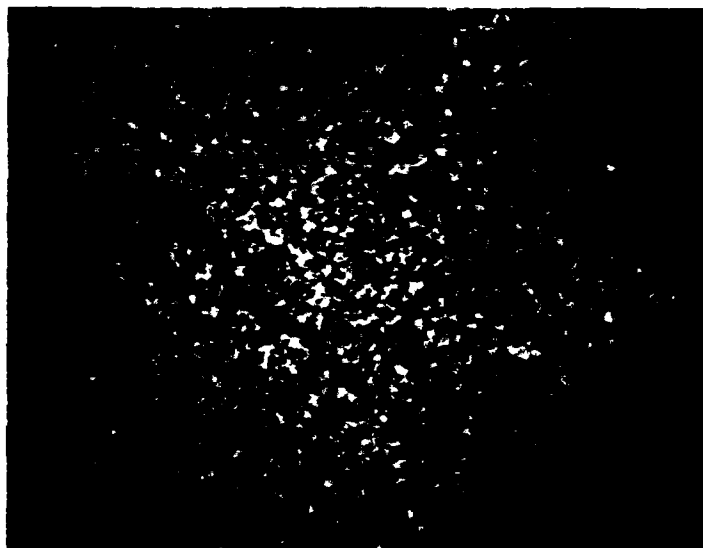
(b.)

Figure 20. 250X Photographs of the Pt Sample Before and After the HTE Test

Silver and Silver on Nickel   The Ag and Ag on Ni
samples appeared bright yellow after the HTE test.
Examination of the samples at 250X showed a very gradual
color change.   However, on black and white photographs the
color change is not obvious and therefore the photographs
were not included in this section.   The compound causing the
color change could not be visually identified.

Platinum on Aluminum   Pt was deposited immediately
after the deposition of the second level aluminum without
breaking the vacuum.   Therefore it was assumed that aluminum
oxide would not be found at the platinum interface and that
the level 2 aluminum would adhere to the level 1 aluminum
oxide.   The top surface of the Pt appeared very similar to
Figure 20a, therefore a photograph of the wafer prior to HTE
has not been included in this section.   Figure 21 contains a
250X photograph of the level 2 Pt on Al after the HTE test.
Once again, there are obvious signs of corrosion.

Platinum on Nickel   Figure 22a contains a 250X
photograph of the level 2 Pt on Ni sample before the HTE
test.   The surface of the top layer of Pt is not as smooth
as in Figure 20a and it appears some type of reaction has
already occurred.   Examination of another level 2 Pt on Ni
sample showed similar results.   Figure 22b contains a 250X
photograph of the level 2 Pt on Ni sample after the HTE
test.   Again, the corrosion has definitely increased.
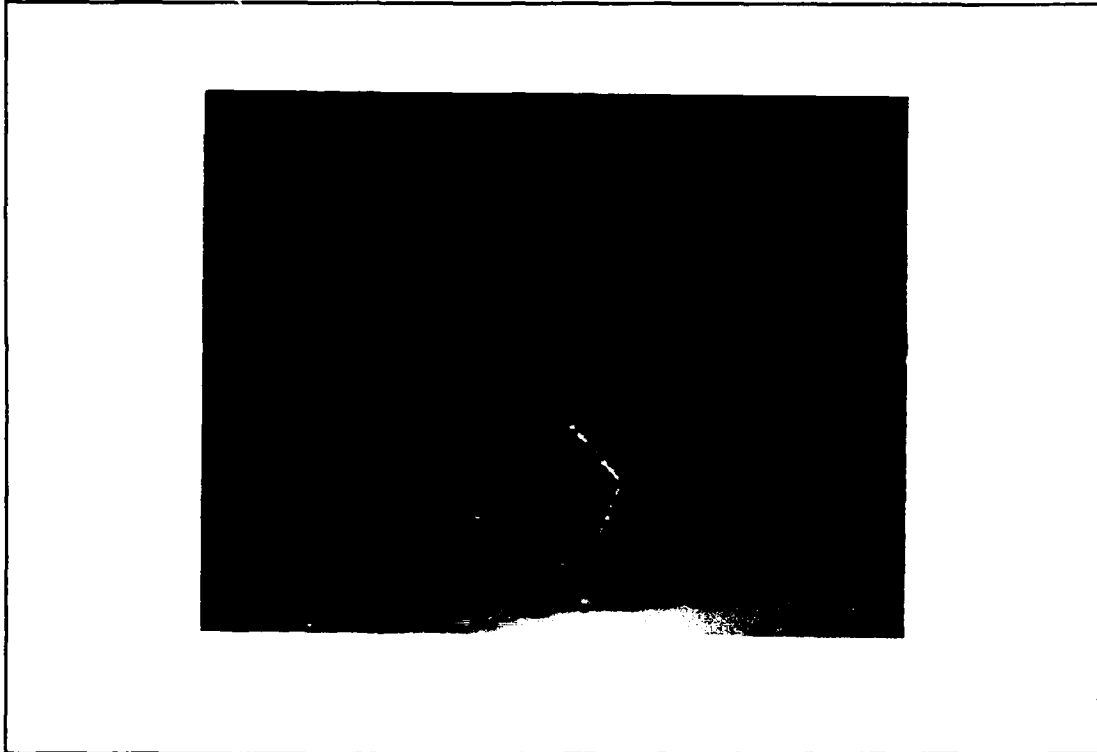
Figure 21. 250X Photograph of the Pt on Al Sample After the HTE Test

Gold on Nickel Figure 23 contains a 250X photograph of the level 2 Au on Ni sample after the HTE test. No apparent signs of corrosion was found. For comparison purposes, Figure 19a is very similar to how the Au on Ni sample appeared before the HTE test.

Electrical Tests Performed

The only electrical test performed was a resistance measurement taken before and after the HTE test. The purpose of this test was to determine if a resistance change
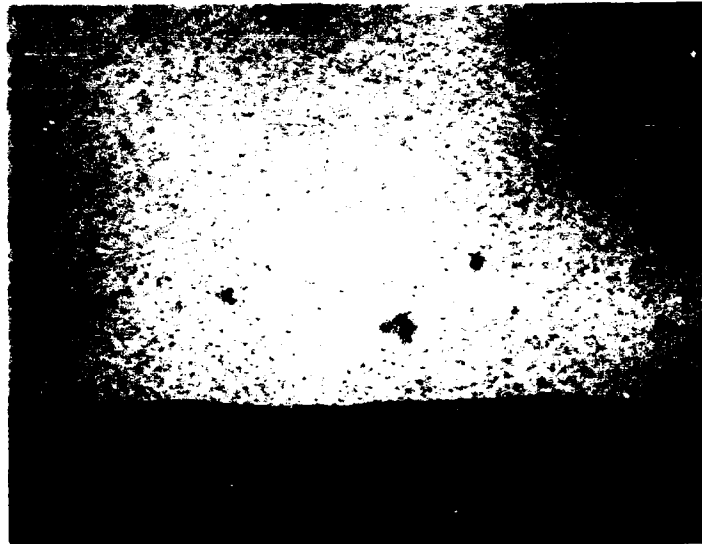
(a.)
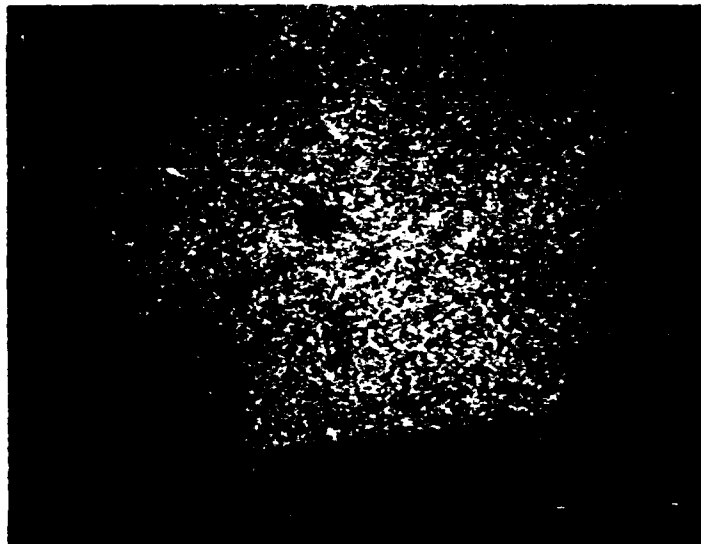
(b.)

Figure 22. 250X Photograph of the Pt on Ni Sample Before and After the HTE Test

1.)   The electrical resistance of the completed metal films were too low to accurately measure. All of the metal film combinations had resistance measurements of 1.1 to 2.0 ohms prior to HTE.

2.)   The thin films of gold and platinum would not adhere to SiO_2. Therefore, an L-shaped thin film structure could not be obtain.

3.)   The films were too thin to allow probing multi-layered films without punching through the top layer of metal. Attempts to obtain thicker films resulted in more temperature problems with the positive photoresist.

VI. <u>Conclusions and Recommendations</u>

The purpose of this chapter is to provide the conclusions and recommendations from the chip test results and the metal study results.

<u>Conclusions</u>

<u>Conclusions from Chip Test Methods and Results</u> The

test results obtained from the redesigned chip only indicates partial success. The modulo-16 four-bit counter does not function. No significant output signals could be detected from any of the counter's four output lines (RA0, RA1, RA2, and RA3). However, if the four outputs of the on-chip counter are physically isolated from the rest of the control circuitry and an external modulo-16 four-bit counter is attached to the four test pads (RA0, RA1, RA2, and RA3), subsequent control circuitry can be tested and verified. Twelve of the sixteen rows of electrodes (ROW_3, and ROW_5 through ROW_15) were selected in the proper count sequence. The operation of three of the sixteen rows of electrodes (ROW_0, ROW_1, and ROW_2) could not be selected as a result of three missing control lines between the selector and row drivers. Therefore, it is not known whether the selector actually functioned for these three rows of electrodes. The

operation of one row of electrodes (ROW_4) was found to be nonfunctional. ROW_4 was always on no matter what the count sequence was. Examination of the CIF plot could not find any obvious errors to account for this problem.

The "on" resistance of the transmission gate contained in the electrode circuitry was found to function as a nonlinear resistor that was dependent upon the applied voltage to the electrode.

<u>Conclusions from the Metal Test Methods and Results</u>

The best way to eliminate the corrosion problem with the aluminum electrode is to deposit a corrosion resistant metal on top of the current aluminum electrode. The corrosion resistant metal must be capable of withstanding the high temperature cure of the polyimide without significantly reacting with the aluminum electrode. The results of depositing the corrosion resistant metal (gold, platinum, or silver) directly on top of the aluminum indicates that a barrier metal is needed to prevent the corrosion resistant metal from reacting with the aluminum electrode during the polyimide cure. The results of using nickel as a barrier metal between the corrosion resistant metal and the aluminum electrode indicate that the gold on nickel combination is the only combination capable of withstanding the polyimide cure temperature without negative side effects. The results of the adhesion tape test indicates that the gold on nickel

combination has excellent adhesion to the aluminum oxide surface of the electrode. Therefore, the gold on nickel combination deposited on the aluminum electrode should not have adhesion problems that could degrade the integrity of the chip from contaminates.

Limitations of Metal Study Test Results The HTE test was performed in a convection oven with an oxygen atmosphere. This is considered a major flaw in the metal study test plan. At 350°C, most metals readily oxidize in an oxygen atmosphere. Further investigation into the polyimide cure procedures contained in previous AFIT theses indicate that the polyimide was cured in an N_2 atmosphere. It is not known how much the N_2 atmosphere would change the previous results.

Recommendations

Recommendations for the Redesigned Brain Chip The redesigned brain chip must have the following deficiencies corrected:

1.) The modulo-16 four-bit counter must be fixed or replaced. The best solution is to replace the counter with a counter design that has already been successfully fabricated and tested for functionality.

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2.) The missing control lines between the selector and row drivers must be replaced. Once replaced, the control circuitry for ROW_0, ROW_1, and ROW_2 must be tested and verified.

3.) The control circuitry for ROW_3 must be analyzed to determine why ROW_3 cannot be selected. Once the error is found, it must be corrected and simulated.

4.) The current two-level aluminum electrode design must be replaced with a single level of aluminum. The single level of aluminum must be the top layer (Metal2) of aluminum in the CMOS description of the circuit. This change will give the electrode the smoothest possible surface.

Recommendations from the Metal Study One of the purposes of this thesis effort was to identify a possible electrode replacement capable of surviving the brain environment and the polyimide curing temperature. The gold on nickel combination provided the most promising results. However, further work is required in the following areas:

1.) A high temperature positive photoresist capable of withstanding the temperatures generated during sputtering is

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needed to mask the gold on nickel combination on the aluminum electrode. The positive photoresist used for this thesis effort produced inconsistent results from one deposition to the next.

2.) The deposition process of the gold on nickel combination must be refined to include the small geometries of the brain chip. This thesis effort made no attempt to sputter any of the corrosion resistant metals on 180 X 180 micron electrodes with a spacing of 70 microns. The photoresist and sputtering processing schedules must be refined to include such geometries.

3.) The HTE test in the metal study should be redone in a N_2 atmosphere in order to simulate the actual polyimide curing procedures.

Implantation of the Brain Chip

The ultimate goal of this research effort is the implantation of the array into the brain of a rhesus monkey. Implantation of the chip is dependent on the results of current research efforts. Obviously, for implantation to occur, the redesigned chip must function properly and the aluminum electrodes must be successfully replaced with a

corrosion resistant metal. Implantation is also dependent on previous research efforts. The preparation of the chip for implantation includes the use of mounting hardware for securing the chip in the brain and processing schedules for polyimide and epoxy, all of which were investigated in previous research efforts. Since the electrical signals from the brain consist of very low voltages in the micro and millivolt range, external amplification circuitry must be designed and implemented. Recording devices are also needed to store the electrical data for further examination. All of the above items must be successfully completed, assembled, and tested before implantation can occur.

Appendix A
Materials and Equipment

Table IX.   Instrumentation

Digitizing Oscilloscope, Model HP 54100
Hewlett Packard Company
Colorado Springs, CO

Fluke Multimeter, Model 77/AN
John Fluke Manufacturing Co
Everett, WA

Keithley 617 Electrometer
Keithley Instruments, Inc.
Cleveland, OH

Zenith 248 Data Collection Computer
(with IEEE-488 GPIB Interface)
Zenith Data Systems,
Glenview, IL

Micromanipulator Probe Station, Model 6200
The Micromanipulator Company, Inc.
Escondido, CA

Micromanipulator, Model 450/360 VM
Manipulators (3),
The Micromanipulator Company, Inc.
Escondido, CA

Power Supply, Model HP 6205B
Hewlett Packard Company
Colorado Sprinrs, CO

Pulse Generator, Model 148
Wavetek, Inc.
San Diego, CA

Aluminum Wedge Bonder, Model TV909
MECH-EL Industries, Inc.
Woburn, MA

Sputtering System, Model DV602
Denton Vacuum
Cherry Hill,NJ

Thickness Monitor, Model TM-100
Maxtek, Inc.
Torrence, CA

Photo-Resist Spinner, Model I-EC101D
Headway Research
Garland, TX

Mask Aligner, Model MJB 3UV300
Karl Suss America
Waterbury Center, VT

Microprocessor Oven(2), Model Imperial IV
Lab-Line Instruments, Inc.
Melrose Park, IL

Micro Ultrasonic Cutter, Model 7000-MUC
The Micromanipulator Co.
Carson City, NV

Microscope with Camera
Wild Heerbrugg Ltd.
Heerbrugg, Switzerland

Surface Dektak Profile Measuring System, Model 9000 50
Sloan Technology Corp.
Santa Barbera, CA

Table X. Materials

Positive Photoresist, Microposit 1350J
Shipley Company Inc.
Whitehall, PA

Hexamethyldisilazane (HMDS)
SCM Corporation
Gainsville, FL

Positive Photoresist Developer, Microposit 351
Shipley Company Inc.
Whitehall, PA

Sulfuric Acid (H_2SO_4)

Methyl Alcohol (CH_3OH)

Hydrogen Peroxide (H_2O_2)

Hydroflouric Acid (HF)

Nitric Acid (HNO_3)

Acetone (CH_3COCH_3)

Chlorobenzene (C_6H_5Cl)

Silicon Wafers

Rubylith
Ulano Corp.
Brooklyn, NY

Kodak High Resolution Photoplates (HRPs)
size: 4" X 4"

Kodak photoplate development chemicals

Appendix B

Processing Schedules

Standard Clean #1 (21:D-1)

The cleaning solution is composed of sulfuric acid (H_2SO_4) and hydrogen peroxide (H_2O_2), mixed in a one to one proportion. It is used to remove organic contaminants from the wafer's surface. The combination of sulfuric acid and hydrogen peroxide results in an exothermic reaction which generates a bubbling action. The reaction lasts only about 15 minutes, after that time the solution is ineffective for cleaning wafers.

The following procedure is done to the wafer prior to oxidation or whenever it is necessary to remove all organic contamination from the wafers:

1. Mix the 1:1 H_2SO_4:H_2O_2 solution in a clean glass beaker and immediately immerse the wafers for 15 minutes. The wafers can be placed in a polypropylene basket for convenient handling.

2. Rinse the wafers in deionized water (greater than 10 Megohms) for 5 minutes.

3. Dip the wafers in a 10:1 HF:deionized water solution for 30 seconds. The hydrofluoric acid will remove an oxide glaze formed by step 1.

4. Rinse wafers in deionized water (greater than 10 Megohms) for 15 minutes.

5. Remove wafers and blow dry with nitrogen gas.

Standard Clean #2 (7:A-1)

The standard clean is performed before the processing of wafers or chips, and this procedure effects the elimination of organic contaminants.

The procedure is:

1. Dip wafers or chips in beaker of acetone to remove organic material.

2. Blow dry with nitrogen gas.

3. Dip in methanol to remove more organic material.

4. Blow dry with nitrogen gas.

5. Flood with deionized water.

6. Blow dry with nitrogen gas.

7. Bake for one hour at $220^{\circ}C$ in N_2 ambient convection oven to remove moisture.

<u>Schedule #1</u> (7:A-2)

This process was used to establish a consistent photolithography process for using 1350J positive photoresist.

1. Clean using Standard Clean #2 process.

2. Preheat second oven to 70°C.

3. Remove wafer from 220°C oven after bakeout and allow to cool.

4. Blow clean with N_2.

5. Apply adhesion promoter (HMDS):

   -puddle on wafer
   -spin @ 5 kprm for 20 seconds

6. Apply positive photoresist (1350J)

   -puddle on wafer
   -spin @ 5 krpm for 20 seconds

7. Prebake photoresist at 70°C for 20 minutes.

8. Blow clean with N_2.

9. Align/expose for 120 seconds.

10. Develop photoresist

    -puddle 351 developer (1:5 with DIW)
    -spin/spray @ 1 krpm for 30 seconds (spray only enough to keep wet)
    -puddle DIW (to rinse and stop developer)
    -spin/spray @ 1 krpm for 30 seconds
    -spin/dry @ 5 krpm for 30 second

11. Examine pattern under microscope, look for fully developed pattern across wafer. If there are any over-developed areas or undercutting, decrease 351 develop time or exposure time.

12. If not fully developed repeat step 10.

Standard Clean #2 (7:A-1)

The standard clean is performed before the processing of wafers or chips, and this procedure effects the elimination of organic contaminants.

The procedure is:

1. Dip wafers or chips in beaker of acetone to remove organic material.

2. Blow dry with nitrogen gas.

3. Dip in methanol to remove more organic material.

4. Blow dry with nitrogen gas.

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    -puddle DIW (to rinse and stop developer)
    -spin/spray @ 1 krpm for 30 seconds
    -spin/dry @ 5 krpm for 30 second

11. Examine pattern under microscope, look for fully
    developed pattern across wafer. If there are any
    over-developed areas or undercutting, decrease
    351 develop time or exposure time.

12. If not fully developed repeat step 10.

Schedule #2

The following procedure was used to generate the photolithography mask previously shown in Figure 17. A design was drawn at 10X scale on a large sheet of rubylith. The pattern used in the metal study consisted of four identical patterns of one square (2000 x 2000 microns) and one rectangle (10,000 x 20,000 microns). Therefore, the rubylith was cut to produce a pattern that was 36 inches square.

The rubylith was then photographed using the mask camera. The reduction multiplier for these masks was 10X. The exposed photoplates were developed using the standard development process. Complete information on the development of high resolution photoplates is available at the AFIT Cooperative Materials and Electronic Processing Laboratory.

Schedule #3

Sputtering was used to deposit all metals in the metal study. All of the metal targets were mounted on a copper target holder with a high temperature conductive epoxy. The following procedure was used to deposit a given metal(s) on a silicon wafer patterned with positive photoresist:

1.   Attach the desired metal target to the sputtering equipment. Insure that all water lines are properly connected to the copper target holder and that the connections do not leak. Input the density, acoustic impedance, and tooling factor into the thickness monitor.

2.   Turn water on to the target and crystal thickness monitor.

3.   Place the patterned wafers in the chamber close the sputtering module.

4.   Pump the system down to less than 1 x 10^{-5} torr.

5.   Turn off the high vacuum gauge.

6.   Open the gas solenoid to allow argon to enter the chamber.

7.   Adjust the needle valve to bring the argon pressure to the desired setting.

8.   After ensuring that the water flow to the sputterhead is on, turn on RF Power on the RFX-600 unit.

9.   Make sure that the power dial is all the way counterclockwise. Press RF ON and bring the dial up so that the forward power is at least 30 watts.

10.   Rotate the TUNING knob on the manual matching network to reduce the reflected power to a minimum. Then rotate the LOADING knob to further reduce the minimum. Repeat if necessary.

11.   Slowly increase the forward power, repeating Step 10 when necessary. When the argon is ignited, a glow is observed in the chamber and the reflected power drops.

12.   Bring the power up (or down) to the desired level. Repeat Step 10 to minimize the reflected power.

13.   Pre-sputter the target for several minutes to remove surface contaminants from the target.

14.   Simultaneously the open the shutter push the START button on the thickness monitor.

15.   Sputter for the desired period of time. To stop sputtering, simultaneously close the shutter and push the STOP button on the thickness monitor.

Appendix C

Report on Counter and Row Selector Design for Robotic

Tactile Sensor

This appendix contains a report written by Capt. Douglas Ford as part of his course work for a VLSI design course at the Air Force Institute of Technology. The report contains design information on a 16 X 16 array intended for use as a robotic tactile sensor. As a result of simuliarities between the robotic tactile sensor and the brain chip, cells such as the counter and row selector contained in the robotic tactile sensor design were used in the brain chip design. The figures in the report were renumbered to agree with the figure numbering of this thesis.

1. BACKGROUND.

Robotic tactile sensor technology is advancing to the point where sensing elements require the spatial resolution similar to that of a human fingertip ($\approx$1mm). One robotic tactile sensor design uses a thin sheet of piezoelectric material to sense an applied pressure at the surface. Beneath the piezoelectric film resides a matrix of MOSFET amplifiers.

In order to achieve this spatial resolution, the tactile sensor incorporates a 16 x 16 MOSFET amplifier array having a total sensing surface area of 6000 μm x 6000 μm. Each sensing element is limited to a surface area of 300 μm x 300 μm, with 100 μm separation between elements. It is impractical (if not impossible) to monitor the output of all 256 elements simultaneously. Therefore, some type of multiplexing scheme is required to acquire the analog output voltages from each sensor element.

2. PROJECT DEFINITION.

This document describes the design for a 16 x 16 sensing array coupled to an analog multiplexing circuit using 3 micron technology. Figure 24 shows the block diagram for the overall circuit. The tactile sensing circuit consists

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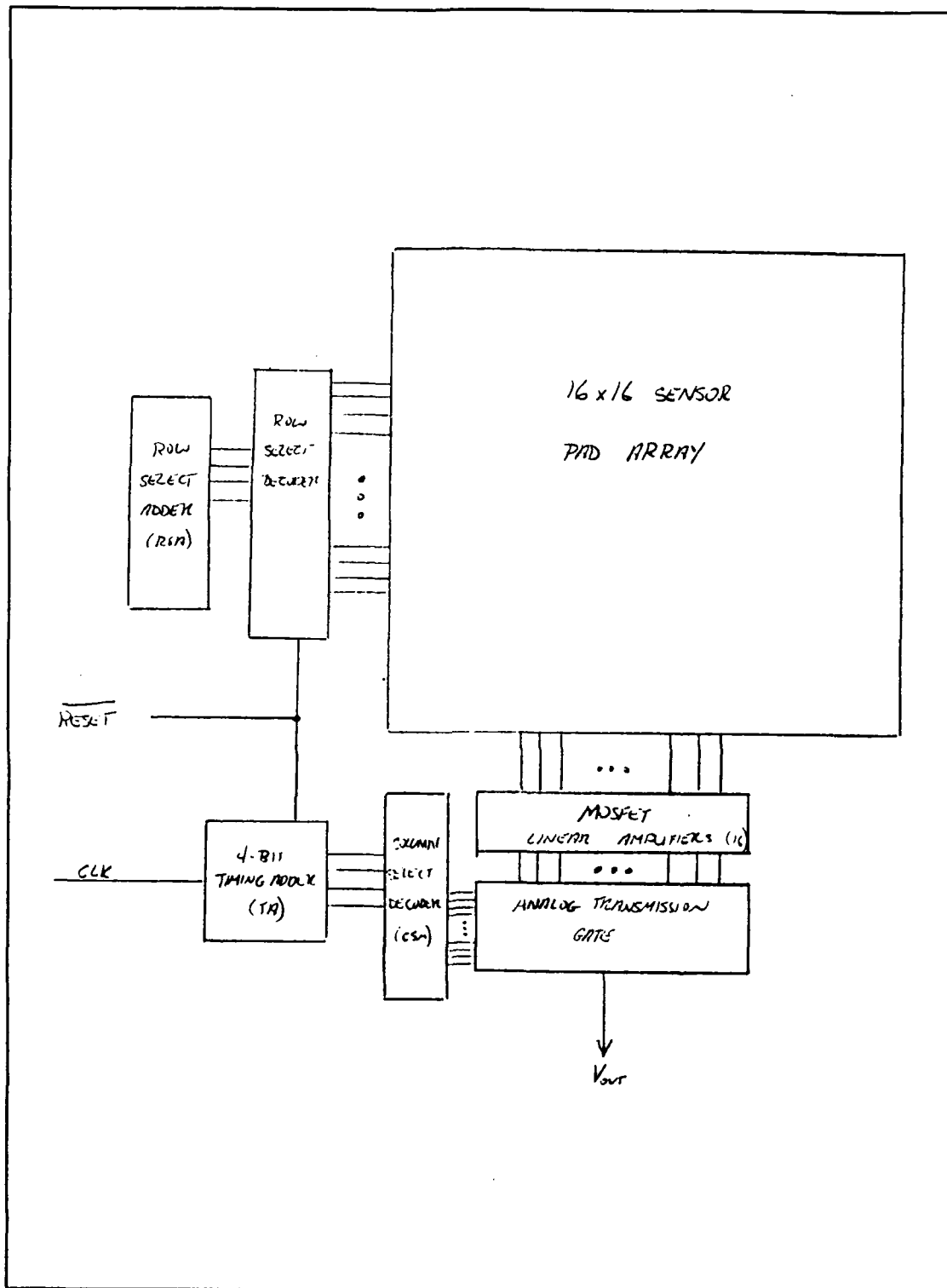
Figure 24. Block Diagram of Tactile Sensing Circuit

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of a 16 x 16 sensing element matrix, a 4-bit binary decoder, and two 4-bit adders. At the base of the sensor array resides a bank of 16 MOSFET linear amplifiers (to be designed). The selected output signal from the tactile sensor multiplexer is fed to an external data acquisition computer using a serial IEEE-GPIB interface.

3. CIRCUIT DESIGN.

Since an array of this magnitude has 256 discrete sensing elements, an electronic analog multiplexing circuit will be included in the IC design to facilitate data acquisition. The multiplexing circuit will require an external clocking source so that maximum operating flexibility may be maintained.

Circuit Operation. Circuit operation begins with an externally applied clock pulse coupled to the input of the timing adder (TA), a 4-bit adder (incrementer). The TA, as shown in block diagram form in Figure 25, consists of four stacked cells, each cell composed of a half-adder coupled to a master-slave D flip-flop. The least significant bit (LSB) input is tied to Vdd, thereby creating the necessary adder input value. The binary value of the output word increases by one each clock pulse. The four output bits couple to the
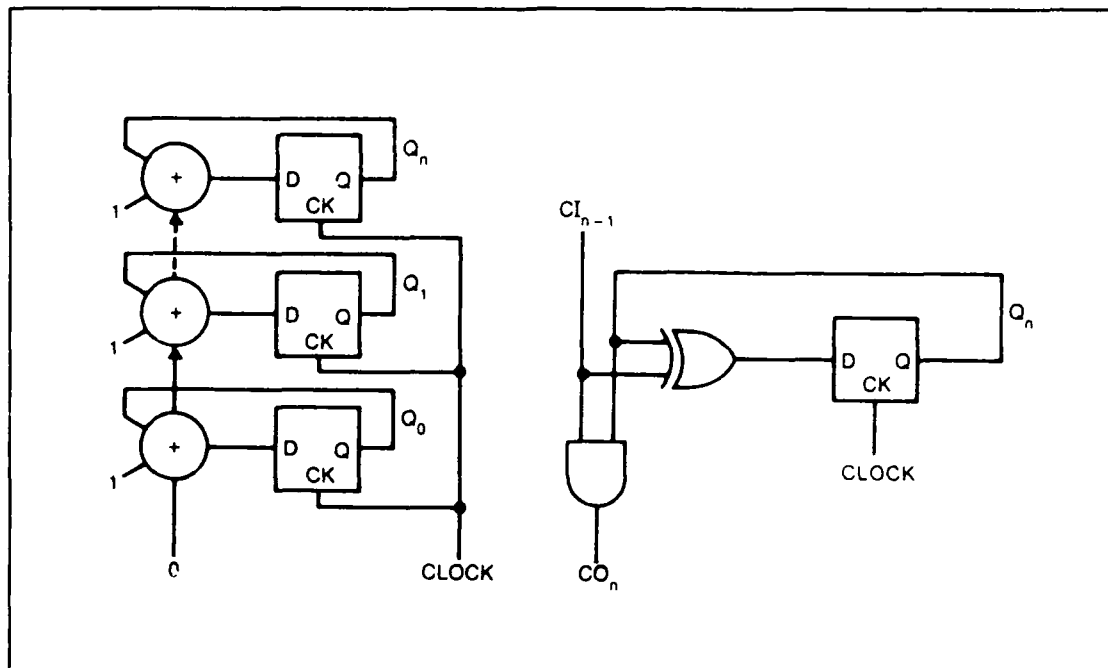
Figure 25. Incrementer Block Diagram (19:338)

column select multiplexer. Q0 defines the least significant
bit, and Q3 is the most significant bit (MSB).

The timing adder's output bits also feed into a four
input NOR gate, constituting a clock signal for the row
select decoder (RSD). When all adder output bits are low,
the NOR gate output goes high. This signifies the last
column is being sampled in the column select multiplexer
(CSM), and the next row must be selected. This process
selects each successive row after completing the scan of the
16 columns.

For each row selected, an analog transmission gate couples the sensor pad potential to the bank of linear MOSFET amplifiers. In turn, the output of each amplifier is routed to a 16 x 1 analog multiplexing circuit. This multiplexer is composed of 16 analog transmission gates controlled by a binary decoder, the CSM. The analog transmission gates used in this project have a predicted input magnitude of 5 V. This implies the pwell contact must be tied to -5 VDC, while the nwell contact is held at +5 VDC. Likewise, the n-type transistor is "turned on" with a gate input of +5 V, and "turned off" with -5 V. The converse situation applies to the p-type transistor.

Simulations. Portions of the above circuit was simulated using the VLSI tools ESIM and SPICE. ESIM is a switch level logic analyzer, mainly used as a digital circuit layout verification tool. SPICE, on the other hand, is a circuit simulation program used typically for linear AC/DC and nonlinear transient analysis of an input circuit.

In this project, ESIM was used to verify design of the incrementer/decoder circuitry. The ESIM output file is shown in Figure 26. With the decoder outputs labeled as R1 through R16, each output is selected sequentially for one clock cycle duration. The Reset input serves as a system initialization input, such that, sensor element (0,0) is the first element to be selected.

```
ICC_DF9X esim12 decoder.sim
224 transistors, 89 nodes (16 pulled up)
sim) I
initialization took 246 steps
sim) I
initialization took 0 steps
sim) h Vdd
sim) l GND
sim) w Clk R1 R2 R3 R4 R5 R6 R7 R8 R9 R10 R11 R2 12 R13 R14 R15 R16
sim) V Reset 001111111111111111111111111111111111
sim) V Clk 010101
sim) V Clkb 101010
sim) G
)010101010101010101010101010101010101:Clk
)1100000000000000000000000000000000:R1
)001100000000000000000000000000000000:R2
)000011000000000000000000000000000000:R3
)000000110000000000000000000000000000:R4
)000000001100000000000000000000000000:R5
)000000000011000000000000000000000000:R6
)000000000000110000000000000000000000:R7
)000000000000001100000000000000000000:R8
)000000000000000011000000000000000000:R9
)000000000000000000110000000000000000:R10
)000000000000000000001100000000000000:R11
)000000000000000000000011000000000000:R12
)000000000000000000000000110000000000:R13
)000000000000000000000000001100000000:R14
)000000000000000000000000000011000000:R15
)000000000000000000000000000000110011:R16
```

Figure 26.   ESIM Output for Decoder Circuit

SPICE was used to determine an optimum size for the analog transmission gates.   The predicted signals passing through the gates was decermined to have a magnitude of ±5 V, with a maximum frequency of 1kHz.   The optimum size for the n-channel MOSFET transistor was determined to be 6 μm long and 25 μm wide.   The p-channel MOSFET transistors was

then 6 μm long and 50 μm wide. The second t-gate configuration had diffusion widths of 10 μm and 20 μm for the n-type and p-type transistors, respectively.

Circuit Layout. Layout of the circuit was accomplished using Magic, a VLSI computer-aided design tool. A 7900 μm x 9200 μm window will be necessary in the final packaged wafer. The vast majority of the area (6000 μm x 6000 μm) is composed of the 16 x 16 sensing element matrix. The final (thesis design) version will include numerous test pads around the periphery of the array to obtain a modular design approach, thereby using nearly all remaining space on the wafer's surface.

The decoder circuitry contains AND-gate drivers that are capable of providing a large enough potential to select all connected AND-gates. The remainder of the circuit is composed of a programmable logic array to select the desired output row (column). The incrementer (counter) circuit consists of half adders coupled to master-slave D flip-flops. The D flip-flop cells are contained in four identical cells.

For the analog transmission gates, the gate inputs from the sensing array columns are routed in from the top of the gate array. Gate selection is determined by the decoder circuit physically located to the left. The output signal

is then routed onto a bus and on to the external data acquisition system.

4. CONCLUSION.

The analog multiplexer circuit used for this robotic tactile sensor will greatly enhance data acquisition capabilities. With 256 probe pads necessary to test each sensor element, significant space on the wafer's surface is saved. A key benefit of using the analog multiplexing circuit is that minimal signal distortion is anticipated. Further analysis will be accomplished following the design of the MOSFET amplifiers.

In addition, by incorporating more test pads, specifically around the incrementer/decoder structures, a great deal more system control flexibility can be obtained. Individual sensor elements may still be probed by electrically connecting these probe pads into the transmission gate control lines leading to specific sensor elements. This is referred to as a modular design approach.

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A 16 X 16 multielectrode array, previously designed in NMOS semiconductor technology and intended for implantation into the brain of a rhesus monkey, must be redesigned in CMOS technology. The multielectrode array, known as the AFIT brain chip, must also have its aluminum electrodes replaced with a corrosion resistant metal that is capable of withstanding a subsequent polyimide cure temperature of 350 degrees Celsius. The possibility of depositing the corrosion resistant metal directly onto the aluminum electrode was investigated. The metals investigated were gold, platinum, silver, and nickel as a barrier metal for the previous three metals. The redesigned CMOS array was partially functional and preliminary results from the metal study indicate gold on aluminum with a nickel barrier between them as the most promising electrode replacement. Further work in this area is continuing.

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